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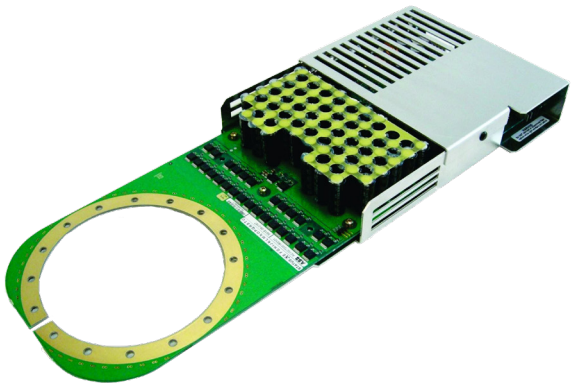
Application note 5SYA 2031-06

Applying IGCT gate units

Nowadays semiconductor manufactures are increasingly taking technical and commercial responsibility for both the power semiconductor and its gate unit. Control parameters such as turn-on and off pulse amplitudes, pulse width and rate of rise, gate circuit inductance, back-porch current and others are standardised by the manufacturer, making the IGCT suitable for converter topologies such as Voltage and Current Source Inverters, Resonance Converters and Static Breakers.



1. Introduction

The control interface discussion between converter design engineers and the power semiconductor manufacturer can be reduced to the specification of power supply, control signal transfer and mechanical assembly leading to a reduction of development costs and time. As a result the power semiconductor technologies made available to a broader group of users. Basic design rules and handling / application recommendations for IGCT gate units regarding power supply, insulation and optical control interface, control-, diagnostics- and protection parameters as well as environmental aspects are described in this application note.

2. Gate unit generations

This application note covers the gate units of several IGCT types. The gate units can be grouped into two generations. Within a generation, the gate units are very similar in circuitry and functionality. They only differ in mechanical size and the dimensioning of the gate drive circuit. The application note is valid for IGCTs with both generation B and generation C gate units unless otherwise noted. Series and parallel connection with different generations is not recommended.

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Table of contents

Table 1 shows the IGCT with its respective gate unit.

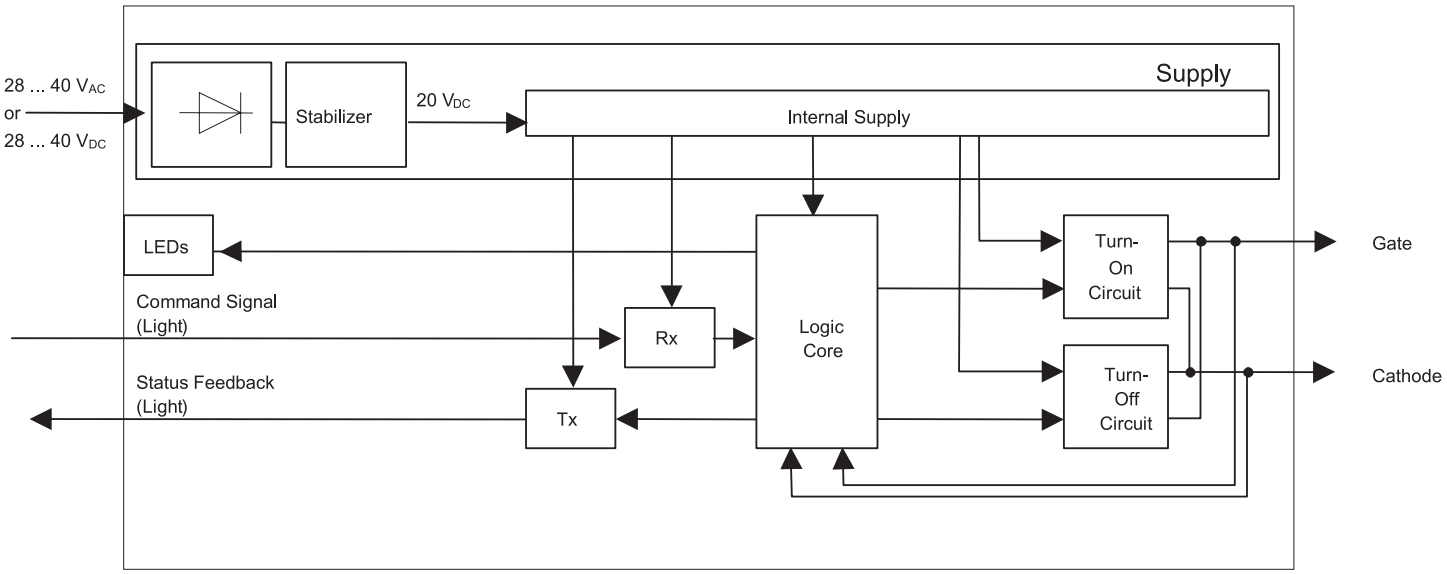
Picture	IGCT types	Gate unit generation
	5SHY 35L4520	B, C
	5SHY 35L4522	
	5SHY 45L4520	
	5SHY 55L4500	
	5SHY 65L4521	
	5SHY 65L4522	
	5SHY 50L5500	
	5SHY 42L6500	
	5SHX 26L4520	
	5SHX 19L6020	
	5SHX 36L4520	
	5SHX 36L4521	

3. Users guide

In this users guide the most important aspects of the gate unit power supply, the insulation interface, the optical interface, control and the diagnostic functionality during normal operation and during fault occurrences are explained. Also environmental issues such as electromagnetic immunity, vibration compliance and thermal management are briefly covered. As an appetizer an example of a functional block diagram of an IGCT gate unit is given in figure 1.

3.1. Power supply interface insulation

The insulation requirement in the IGCT environment is a function of the maximum applied nominal voltage of the converter application itself. This voltage varies from a few thousand volts to several tens of thousands of volts over the IGCT application range. Hence, the requirements on insulation strength and distances can be very different. Furthermore, the power which needs to be transferred through the insulation interface is also strongly application dependent, and users are likely to require quite different insulation interfaces in terms of both power handling capability and insulation strength. As this also applies to the costs of the interface, standardisation of the insulation interface is difficult. This is why the IGCT gate unit does not provide an on-board potential separation. The gate unit power supply output as well as the supply cable must withstand the high voltage potential of the power semiconductor switch against all other relevant potentials in the converter.



01 Block diagram of an IGCT gate unit

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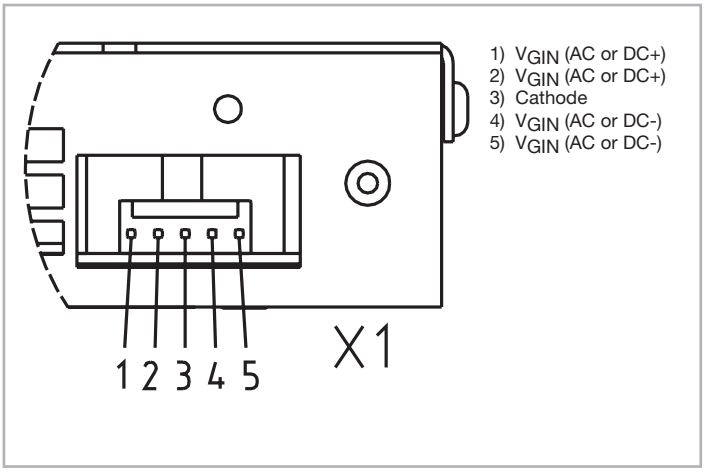
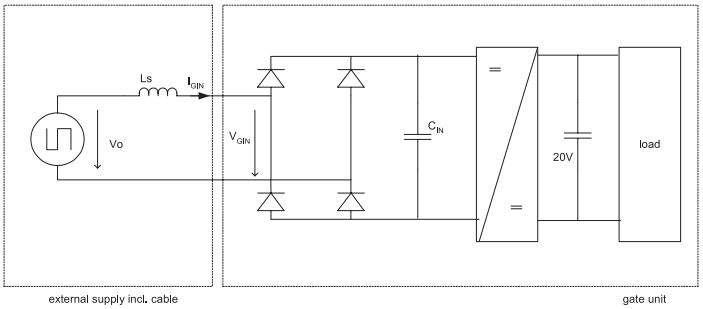
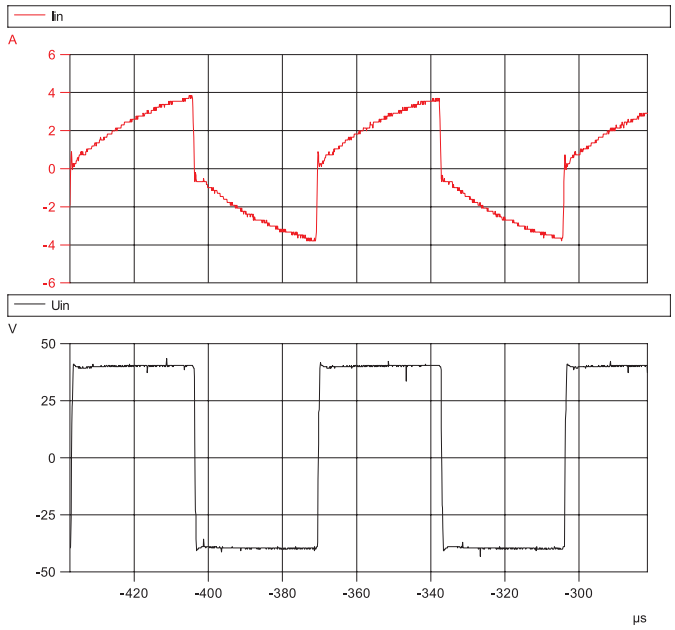


02 Pin layout of power input connector X1 (looking into the connector from the outside)



03 Principle circuit of gate unit input stage



04 Typical waveform of input voltage and supply current when using square-wave AC supply

Gate unit power connector

The connector X1 (figure 2) is specified in the corresponding IGCT data sheet. Information about the corresponding power cable connector can be found on the connector supplier's website, which is also mentioned in the data sheet.

Input voltage, input current

The gate units have built-in rectifiers and voltage regulators. Hence the insulation transformer output can be connected directly to the gate unit power supply input. It is also possible to supply the gate unit with a DC-Voltage. The input voltage of the gate unit $V_{GIN,RMS}$ has to be within the range specified in the data sheet. Note that only square-wave AC-voltage is specified. Do not use a sinusoidal AC-voltage for the supply.

Figure 3 shows the principle of the input stage. When voltage is applied, the capacitor C_{IN} is charged. After a delay of about 3 s the internal voltage regulator starts to charge the large capacitor bank. The voltage regulator limits the charge current to $I_{GIN\ Max}$ (see data sheet).

When supplying the gate unit with AC-square wave voltage, the following items have to be considered: The supply itself and the supply line always contain some stray inductance. As a consequence of this stray inductance, the supply current will have a saw tooth shape as shown in figure 4.

The current slope results in a voltage drop across the stray inductance. When power is transferred to the gate unit, the source voltage has therefore to be higher than the minimum required gate unit input voltage $V_{GIN,RMS}$, howeve, it must not be higher than the maximum allowed input voltage for quiescent operation. With the following formula the required source voltage can be calculated:

$$V_0 = V_{GIN,RMS} + \frac{8 \cdot P_{GIN} \cdot Ls \cdot f}{V_{GIN,RMS}}$$

with

V_0 required source voltage

$V_{GIN,\ RMS}$ minimum supply voltage according to data sheet

P_{GIN} gate unit power consumption

Ls stray inductance of the AC power supply in cluding the supply cable

f frequency of the AC power supply

This calculation is valid for a square wave without dead time.

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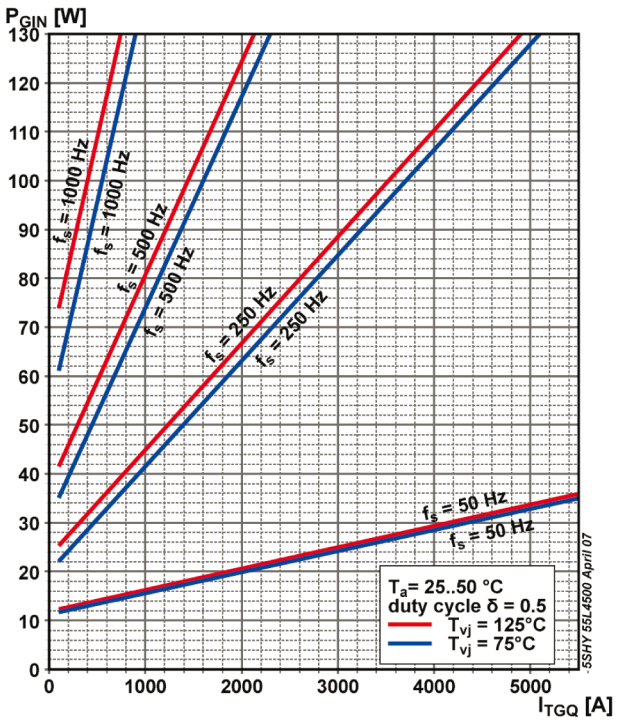
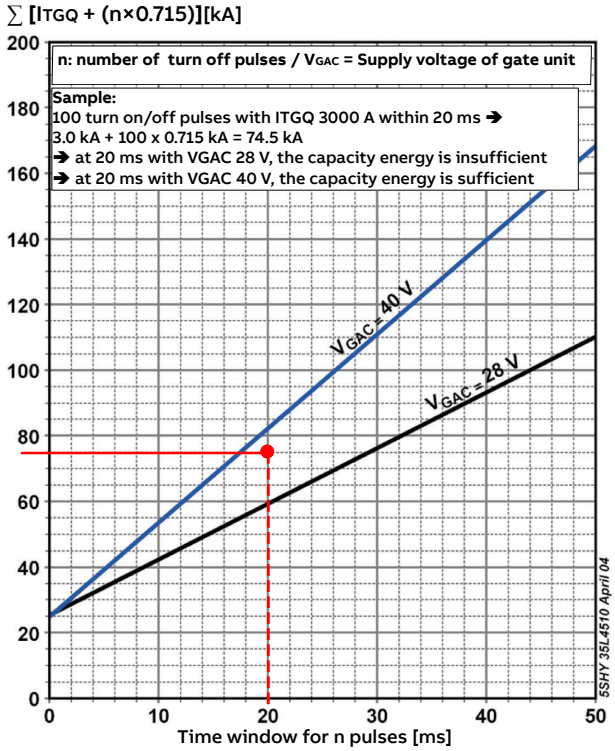


05 Maximum gate unit input power (dissipated plus transferred) in chopper mode, example of a gate unit generation B



06 Burst capability of gate unit

AC square wave supplies are often equipped with a pulse-to-pulse current limitation. This current limitation has to be adjusted to a value higher than the peak supply current which can be calculated with the following formula:

$$\hat{I}_{GIN} = 2 \cdot I_{GIN} = 2 \cdot \frac{P_{GIN}}{V_{GIN,RMS}}$$

with

$\mathbf{V_{GIN,\,RMS}}$ minimum supply voltage according to data sheet
$\mathbf{P_{GIN}}$ gate unit power consumption
$\mathbf{\hat{I}_{GIN}}$ peak value of the supply current
$\mathbf{I_{GIN}}$ rectified average value of the supply current

During power-up a minimum rectified average current $I_{GIN\,Min}$ has to be supplied. This current may be lower than the internal current limitation of the gate unit. However, to avoid start-up problems and breakdown of the power supply voltage it is recommended to use a power supply that is able to deliver at least the value of the internal current limitation $I_{GIN\,Max}$ of the gate unit specified in the data sheet.

Power Consumption

The total power consumption of the IGCT gate unit is strongly load dependent as can be seen in figure 5. The turn-off current I_{TGQ}, the switching frequency f_S, the silicon temperature T_{vj} and the device technology (determining the gate charge Q_{GQ}) have a major influence on power consumption. The bulk of the power though, is transferred to the GCT with only a small part of it being dissipated in the gate circuit itself. Nevertheless, gate unit limitations must be checked before the operating range in a specific application is determined. For thermal limitations see figure 20.

Burst capability

In some operation modes, the IGCT should commutate a number of high current pulses. The gate unit includes a significant capacitor bank to provide that capability. Since the energy capacity of the gate unit and its supply is limited, certain limitation occur for triggering. The capability to generate a number of pulses within a certain time window is defined by the switching current I_{TGQ} and the model specific factor found in the data sheet.
The following factor is calculated to prove the gate unit capability for this specific operation mode.

$$\sum \left[I_{TGQ} + (n \times 0.715) \right] [kA]$$

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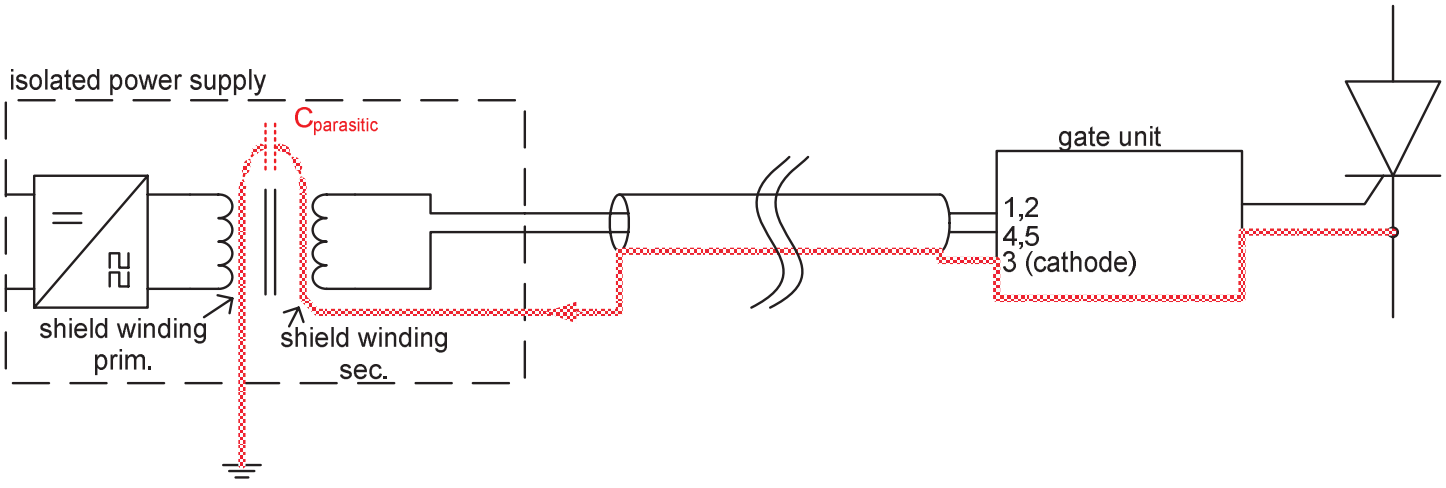
See below a sample to verify the capability of commutating 100 pulses (n) of switching current of 3 kA (I_{TGQ}) within a time window of 20 ms for a IGCT with a model specific constant of 0.715 kA.
Process:
1. Calculate the current factor 3 kA+ (100 x 0.715 kA) = 74.5 kA
2. Verify the calculated factor of 74.5 kA within the diagram (e.g. diagram item 6)
a. Select the graph of the gate unit supply voltage V_{GAC}
b. Verify, that the value is equal or less to the graph at the time of the time window's value

In the given sample, the capability is given for V_{GAC} = 40 V, but is insufficient for V_{GAC} = 28 V
Remarks: Ensure the minimum times for t_{on} and t_{off} are maintained to disable undesired retriggering. Furthermore the thermal effects must verified to avoid the device overstress due to exceeding of junction temperature limits T_{vjMax} generated by the switching losses of the GCT during this operation mode.

Shielding of the insulation transformer
Insulated power supplies and transformers always have a parasitic capacitance between input and output. This capacitance produces common mode displacement currents through the power supply line during voltage jumps. The gate unit is robust against these currents, however it is recommended to minimize them. This is especially important for applications with series connected devices where higher dv/dt referenced to ground occur.
There are several possibilities to reduce such parasitic currents:
• Minimize parasitic capacitance of the power supply.
• Feed the supply line through a ferrite core. This will reduce the peak amplitude of the displacement current and also reduce its rise time, thus relieving the strain on the gate unit.
• Use transformers with shielded windings. The gate unit supply connector has a pin that is directly connected to the housing (cathode). This pin can be used to carry the displacement current and bypass it to the cathode. Figure 7 shows the principle of this method.
The displacement current is bypassed through the red marked path to ground and does therefore not flow through the sensitive electronics on the gate unit board. The connection from the isolated power supply to the IGCT is ideally made with a shielded cable using the shield to connect the secondary shield winding of the transformer with the gate unit.

Start-up behaviour of gate unit Generation B
The IGCT starts up around 3 seconds after supplying with power. During start up it consumes a high peak current and the voltage V_{GIN} may dip below 28 V. A voltage dip which doesn't meet the mask requirement in figure 8 (and figure 9), may damage the IGCT or a malfunction occurs. The voltage V_{GIN} must be measured directly at the power input connector X1. For AC-Operation a scope with mathematic functions must be used. The absolute value from the voltage V_{GIN} is to filter. The -3 dB frequency of the low pass filter should be at least 1.5 kHz. This method calculates the theoretical DC value of an AC square wave.

Start-up behaviour of gate unit Generation C
After supplying the IGCT with power the logic will start up and LED status will be visible. Around one second later the main power supply will be turned on and the big capacitor bank will be charged up. The soft start functionality prevents the IGCT to consume a high peak current during start up.
External power supply must deliver I_{Ginmin} and V_{GinRMS} must be in the defined range, to guarantee a safe start-up of the IGCT.



07 Principle of using the shield to reduce parasitic currents

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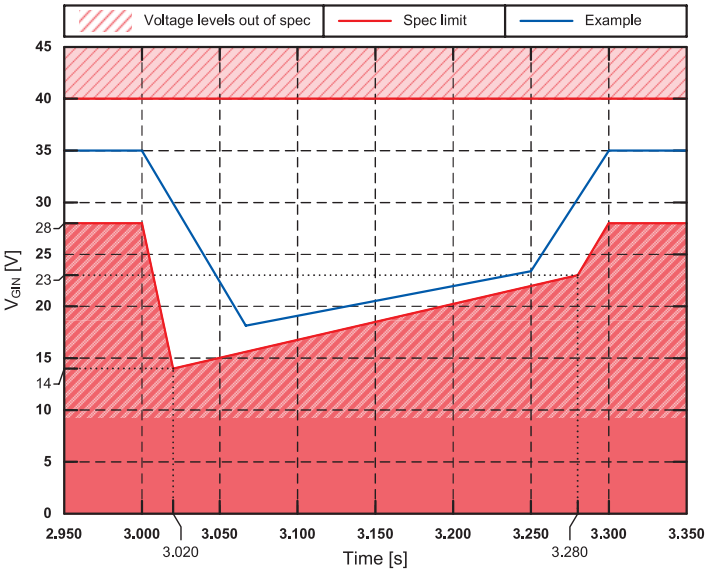
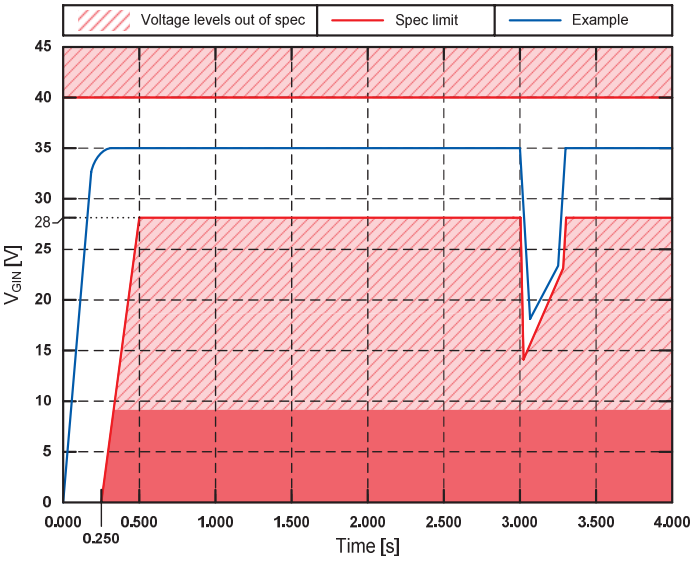


08 Mask for allowed voltage dip during gate unit start up



09 Gate unit start up

3.2. Optical interface

The optical control interface uses standard components, which are widely used throughout the industry. It is built up around the HFBR-1528Z / HFBR-2521Z of Broadcom Technologies (www.broadcom.com), operating at 650 nm. The recommended standard type optical fiber is 1 mm POF (Plastic Optical Fiber), which gives a cost-effective and easy-to-use solution. For long distances (> 15 m) the 200 µm HCS type (Hard Clad Silica) type is recommended (optional feature, please contact HCS factory). One of the most sensitive parts of the gate unit is the optical Interface. Strict adherence to the mounting instruction (chapter 4.5) is highly recommended to inhibit faults.
The specific optical data are given in the data sheets of the IGCT products and on the supplier's website.

Driver circuit

The receiver used on the gate unit is optimized for fast response times and low pulse width distortion. However it is not only sensitive to the level of the optical power but also to the rate of change of the optical power. Therefore the driver circuit has to be designed carefully to avoid unforeseen behaviours of the optical link. A recommended driver circuit can be found in the Avago Technologies transmitter data sheet. Other circuits may be possible but the following issues have to be observed:

- The transmitter current should be rectangular. A turn-on overshoot of the current should be avoided since this can lead to erratic behaviour of the receiver.
- The supply voltage should be properly filtered in order to avoid ripple on the transmitter current.
- If the transmitter is not driven by a push-pull stage, a discharge resistor directly across the transmitter diode is needed to achieve a fast turn- off edge
- Loop areas in the driver circuit should be minimized in order to avoid that noise is modulated onto the transmitter current by electro-magnetic fields.
- The driver circuit should be fast enough to achieve rise and fall times of the transmitter currents below 100 ns.

Optical power

It is essential that the specified optical power is maintained. The receiver data sheet allows a lower optical power level than the level specified in the IGCT data sheet. However, the IGCT is normally used in an environment with very harsh electromagnetic noise. Therefore, the optical power has to be large enough to provide a sufficient signal to noise ratio. Too low optical power can lead to unforeseen switching occurances in combination with electromagnetic noise. The specified optical power levels for the command signals are referenced to the input of the gate unit's receiver. It is recommended to measure the optical power prior to the commissioning of the system. A suitable device for this measurement is the optical meter «OP850LD650-SI3-VL from Opto Test (www.optotest.com).
When designing driver current, the aging of the transmitter and the optical link also have to be taken in account, otherwise failures may occur after years of operation.

States of the command signal to be strictly avoided

Any optical power level between $P_{on\ CS}$ and $P_{off\ CS}$ should be strictly avoided (except of course during the switching transition). Such power levels may lead to arbitrary switching of the gate unit with almost unlimited frequencies. This may damage the gate unit or the GCT. Common situations in which such power levels might occur

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are:
• Connecting or disconnecting of the optical fiber while the command signal is on.
• Powering the gate unit without fiber attached on CS and without a dummy plug in the receiver (stray light).
• During power up and down of the control board. The control board has to be designed carefully to avoid the gating of the transmitter driver before its power supply voltage is within its operating range and the transmitter therefore is operated with insufficient current. If this is not possible it is necessary to power the control board prior to the gate units and vice versa during power down. However, keep in mind that the gate unit has a large capacitor bank and might therefore be operative more than 10 sec after turning off its power supply.

How to lay the fiber optic cable
Careful laying of the fiber optic cables is important. Some basic rules have to be observed in order to avoid additional attenuation of the optical link power.
• Avoid sharply bending. A bend radius below 35 mm should be avoided.
• Do not tighten cable retainers too firmly.
• Avoid proximity to hot surfaces (e.g. power resistors) for this may accelerate the aging of the fiber.
• Avoid tensile load on the fiber.

3.3. Control aspects signalling

The IGCT requires a command signal from the converter control part and transmits in return a status signal. In normal operation, the gate unit translates the command signal as follows:

Light = IGCT ON
No light = IGCT OFF

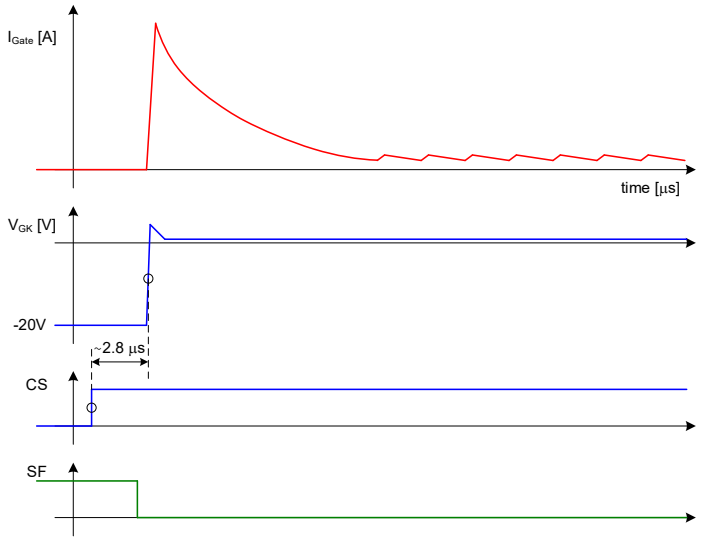
Power-up of gate unit power supply
Any attempt to turn on the IGCT before the power-up sequence is completed may cause a power-up failure or even the destruction of the gate unit. It takes up to 5 seconds from the start of the power-up until the gate unit is ready for operation. Since the gate of the GCT has to be negative biased in order to have the full blocking capability, the blocking capability is reduced until the gate unit is fully powered -up. Therefore, we recommend always powering-up of the gate unit before voltage is applied on the IGCT. During power up of the IGCT SF should be ignored.

Glitch filter
A glitch filter suppresses noise spikes appearing on the optical input. All pulses with a pulse width t_{glitch}, smaller than

$t_{glitch} < 400$ ns

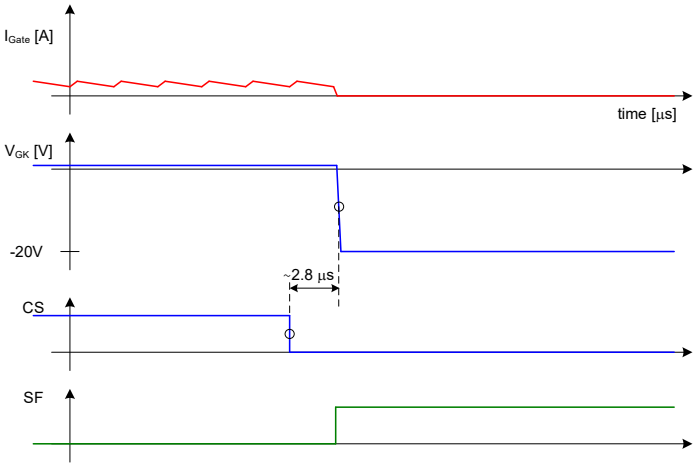
are ignored. This applies both to the ON and OFF state.

Turn-on delay time (figure 10)
The typical gate unit turn-on delay time is 2.8 µs (50 percent change of light Command Signal (CS) to 50 percent change of gate-cathode voltage - V_{GK}). It is slightly smaller than the overall IGCT turn-on delay time t_{don}, which is specified in the corresponding IGCT data sheet.



10 Turn-on delay (measurement)

Turn-off delay time (figure 11)
The typical gate unit turn-off delay is 2.8 µs (50 percent change of light Command Signal (CS) to 50 percent change of gate-cathode voltage - V_{GK}). It is much smaller than the overall IGCT turn-off delay



11 Turn-off delay (measurement)

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time t_{doff}. Further data can be obtained from the specific data sheet.

Minimum ON and OFF pulse widths

The minimum possible pulse width given by the gate unit is smaller than the minimum ON or OFF time the IGCT requires. t_{ONMIN} and t_{OFFMIN} of the relevant IGCT data sheet have to be observed.

Refiring during on-state

A negative gate bias during on-state is a cumbersome mode of operation for IGCT and GTO gate units. This mode occurs in any VSI circuit when an anti-parallel freewheeling diode is conducting; i.e. the switch current is negative. Firstly, in this mode the power dissipation in the gate unit increases. Secondly, the gate current flows through the anode and not through the cathode where it should flow. Thirdly, at the zero crossing of the switch current, the GCT is not quite ready for conduction and anode voltage is built up before latching takes place again. A so-called «power pulse» which is the product of the transient voltage and current pulse can be observed on the oscilloscope. It is not the magnitude of the power pulse, which is harmful, but the accompanying inhomogeneous current distribution in the semiconductor, which may lead to device failure if «power pulses» are generated in a repetitive mode and nothing is done to suppress them. IGCT gate units have features to ensure robust and reliable operation in the negativebiased on-state mode:

a) Detection of gate-cathode voltage polarity V_{GK}

b) Reduction of gate current when the gate to cathode junction is negatively biased (freewheeling diode is conducting)

c) Automatic re-execution of turn-on pulse (called internal re-trigger) when the gate to cathode voltage V_{GK}, becomes positive again

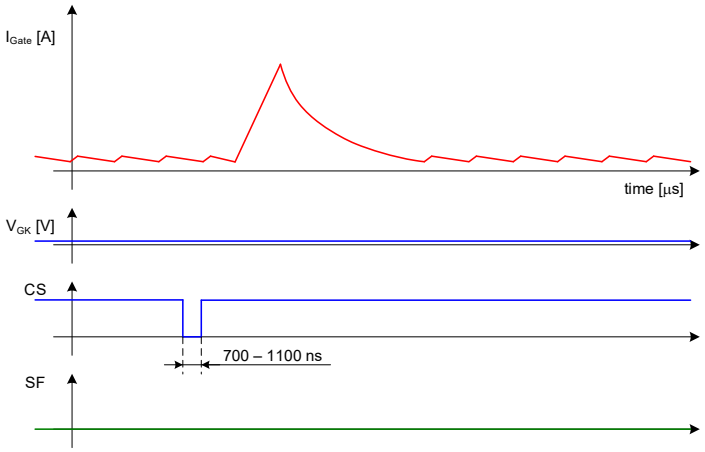
d) External re-trigger of the turn-on pulse during on-state

Features a) – c) are sufficient to handle freewheeling diode conduction in topologies with «normal» di/dt values typically caused by the zero crossing of an inverter phase output load current of less than 50 A/µs. However, in some applications the internal re-trigger may be too slow. This is for example the case if a high di/dt current pulse is applied to an IGCT switch in a freewheeling diode conduction mode or very low anode current conduction (quiescent mode).

For such extraordinary cases, the external re-trigger feature was implemented. The external re-trigger command is executed when a turn-off pulse (no light) with a pulse width between 0.7 and 1.1 µs is applied to the optical input interface. Shorter OFF-pulses are ignored (glitch-filter) and longer OFF-pulses lead to a minimum OFF pulse of 3.5 µs. Figure 12 shows an example of an external re-trigger command. The turn-on circuit is thermally designed for a maximum frequency of 2000 Hz (turn-on plus retrigger pulses). Due to internal gate unit conditions an additional restriction applies to the use of the re-trigger function:

Earliest re-trigger after turn-on: > 20 µs

For obvious reasons the re-trigger command can be executed during on-state only. The additional power required for the retrigger pulses is already accounted for in the power consumption diagram (figure 5).



12 External re-trigger (measurement)

Operation of the IGCT without gate unit power supply

Since the gate of the GCT has to be negative biased in order to have the full blocking capability, the blocking capability is reduced when the gate unit is not powered. Negative voltage, even the on-state voltage of the anti-parallel freewheeling diode, should be avoided when the gate unit is not powered, because this could damage the gate unit.

3.4. Diagnostics / Protection status feedback

The gate unit provides an optical status feedback output (SF) signalling either OK or FAULT.

OK:

- In normal operation, the optical status feedback signal is inverse to the command signal.

FAULT:

- Supply voltage fault (over-/ under-voltage): The feedback signal is in phase with the command signal.
- Gate-cathode short circuit (failed IGCT): The feedback signal remains off.
- Output does not follow input (other fault): The feedback signal is dependent on the fault condition signal.

Most GCT failures eventually lead to a gate to cathode short circuit. However the impedance of the gate unit's turn-off circuit is very low. It therefore requires a really low short circuit impedance to make fast detection possible. It is therefore possible that a turn off failure

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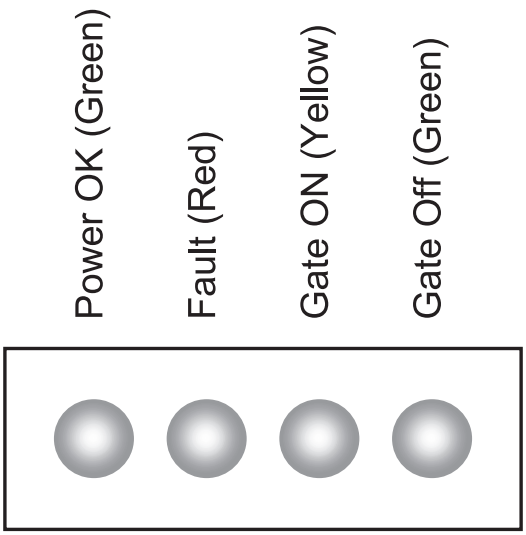
may not be detected by the gate-cathode monitor. In this case, the supply voltage monitor does detect the failure. However, this may take several hundreds of µs until the status feedback signals this state. Under normal operation the status feedback signal follows the cs command signal with a maximum delay of 7 µs.

Visual Feedback

The gate unit is equipped with visual feedback information, which



13 LEDs for visual feedback

indicates the status of the IGCT (figure 13).

Diagnostics status table

The optical status feedback output (SF) and the four LEDs (see figure

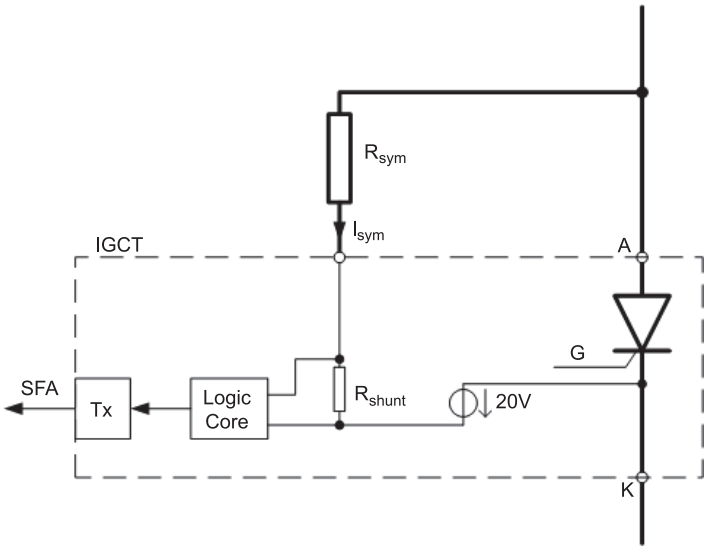
LED	Color	Description
Power OK	green	internal capacitor bank voltage okay [3]
Fault	red	- internal capacitor bank voltage out of range - gate voltage not in correlation with comand signal - gate cathode short circuit [4]
Gate ON	yellow	- gate current flowing
Gate OFF	green	- off channel active

Table 2

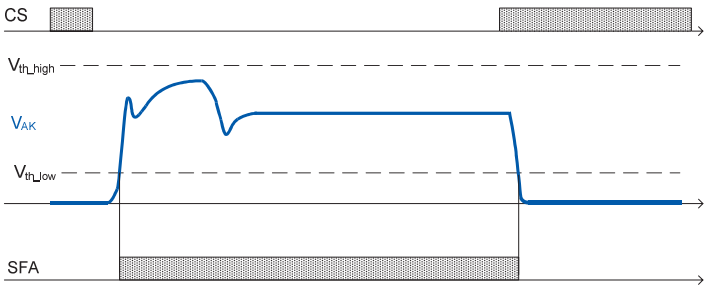
[3] For gate unit generation B: Internal capacitor bank and input voltage okay

[4] Gate unit generation A: flashing

13) provide the user with information according to the table below: Re-trigger action does not influence or change the optical status feedback or the visual feedback.



14 Principle of anode voltage monitoring



15 Normal operation

Anode voltage monitoring (optional feature)

The gate unit generation B has the option of anode voltage monitoring. This feature is useful to detect if the device and its freewheeling diode is blocking when IGCTs are series connected. There is also the possibility to detect overvoltage across the device due to voltage misssharing. To monitor the anode voltage, a high voltage resistor has to be connected between the gate unit and the anode. This resistor can at the same time be used as a balancing resistor. The feedback for the anode voltage monitoring uses a separate fiber optic transmitter. Note that the anode voltage monitor feedback signal is not filtered. The conditioning of the signal is up to the user. Independent of other gate unit states, the anode voltage status feedback (SFA) has the following functionality:

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	Anode voltage feedback (SFA)
$I_{sym} < I_{sym,\ th,\ low}$	no light
$I_{sym,th,low} < I_{sym} < I_{sym,\ th,\ high}$	light
$I_{sym} < I_{sym,\ th,\ high}$	no ligh
Gate unit not supplied	no ligh

with $I_{sym,\ th,\ low} \cong 16.5$ mA and $I_{sym,\ th,\ high} \cong 75$ mA

The voltage threshold levels are dependent on the resistor R_{sym} and can be approximated as follows:

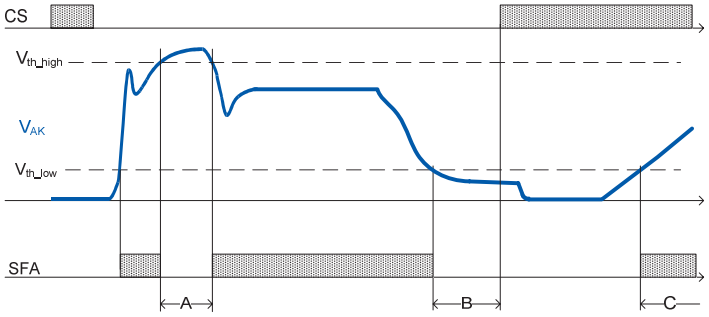
$$V_{th} \cong I_{sym,th} \cdot R_{sym} - 20V$$

Please contact factory for design support. Example:
Rsym = 60kΩ

$$V_{th,low} \cong I_{sym,th,low} \cdot R_{sym} - 20V \cong 970V$$

$$V_{th,high} \cong I_{sym,th,high} \cdot R_{sym} - 20V \cong 4480V$$

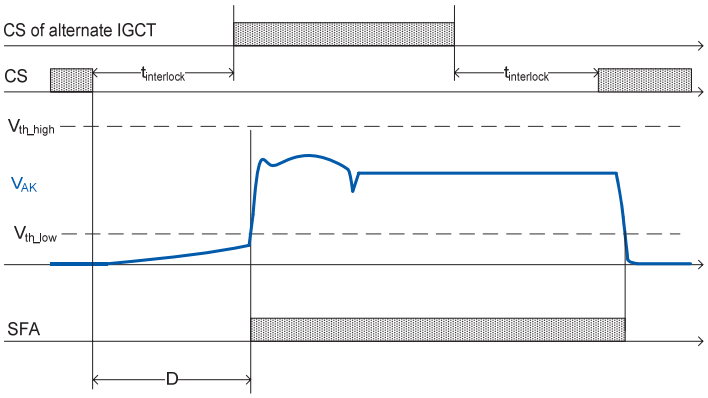
Where $V_{th,\ low}$ and $V_{th,\ high}$ can be seen in figures 15 and 16.



16 Fault conditions

A) Overvoltage during off-state (e.g. caused by voltage miss sharing or dynamic voltage overshoot due to switching)
B) Undervoltage during off-state (e.g. due to failure of GCT or free-wheeling diode)
C) Voltage applied during on-state (e.g. broken fiber optic link of command signal)

The anode voltage status feedback is not filtered in the gate unit in order to forward as much information as possible to the user and therefore allowing for an individual and flexible adaptation to the application. The anode voltage monitoring feature seems to be useful to detect if a GCT or its antiparallel diode has failed during turn-off in order to avoid turning on another IGCT. However, if the GCT is carrying a low current or if its antiparallel diode is conducting, then the voltage across the GCT will rise only slowly or not at all until an alternate IGCT turns on and forces the voltage to rise (see figure 17). At this moment it is already too late to avoid a shoot-through. A slow rise of the voltage is particularly pronounced with a snubber across the IGCT. As the IGCT does not always build up voltage when it is switched off, an electronic control system is required to identify the state of the IGCT current in order to initiate corrective actions due to the anode voltage status feedback.



17 Turning off low current

Protection
A detected fault condition will invert the status feedback signal (SF) and turn on the fault LED. With few exceptions the gate unit will follow the command input (CS) as a slave even under fault conditions. A GCT fault detection, is not possible when the IGCT is in on state mode (CS = on).

- Loss of power supply
When the power supply is lost, the slave function of the gate unit can be guaranteed as long as the logic supply voltage is sufficient. After that, the last valid command status will be frozen. Hold up times can be guaranteed as follows:
On state hold-up time (no switching): > 200 ms Off state hold-up time (no switching): > 500 ms

- Open gate circuit
We strongly advice not to energize the gate unit without having the GCT-part mechanically clamped. This may damage the gate unit components and the GCT when the gate current source is working into an open circuit.

- Shorted gate circuit
A shorted GCT (only when CS = off) forces the internal supply voltage to zero and drives the voltage regulator into current limitation.

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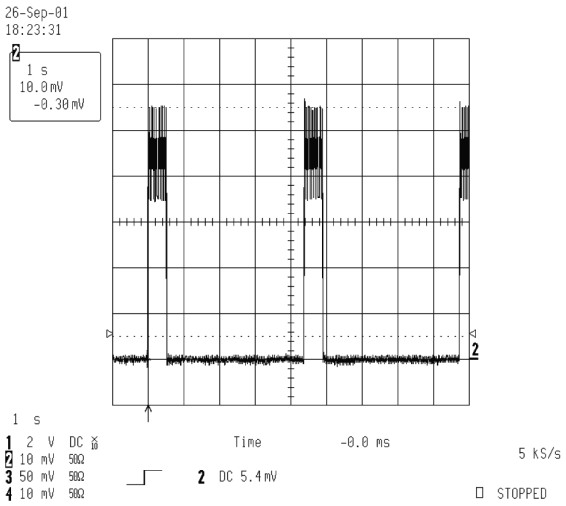
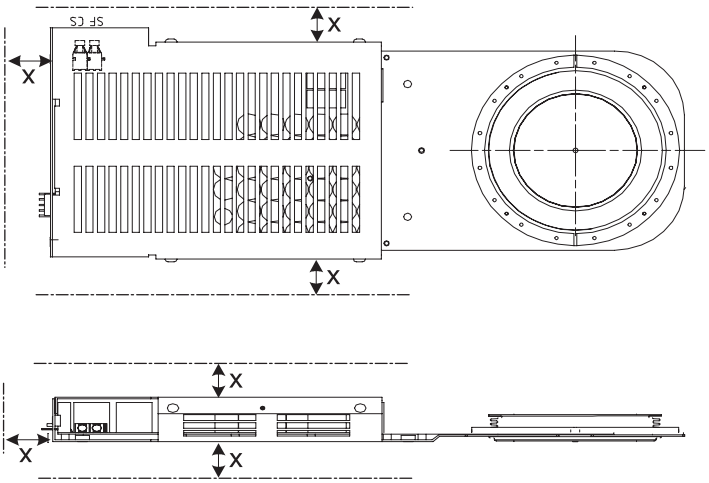


18 Power up during shorted gate unit load



19 Distance between gate unit and parts with high di/dt

To prevent overheating, the power supply is separated from the gate unit after some hundred milliseconds. After another 4 to 5 seconds the power supply tries to power-up the gate unit again. This will only be successful if the gate-to-cathode short has been removed. In case of a sustained short circuit, the power supply will «pump» current into the short circuit as shown in figure 18.

3.5. Environmental aspects, Electromagnetic Immunity (EMI)

The dominant EMI stress on the IGCT gate unit stems from the gate unit itself and the noisy converter switching environment. The noise generated in the gate unit itself comes from high di/dt turn-on and turn-off pulses, whereas the switching environment typically produces

• high di/dt repetitive switching and surge transient currents flowing in bus bars, cables and di/dt chokes.
• high dv/dt potential shifts within the stack construction (heat sinks, clamping equipment) and between stack components and equipment grounding potential.

Immunity type tests are done at the following conditions to simulate the worst cases of the above phenomenon:
- dv/dt stress: > 20 kV/µs with amplitude 4 kV
- di/dt stress: 5 kA/µs with amplitude 7 kA
- magnetic field: 150 A/µs with amplitude 40 kA applied in a coil with 9 windings, diameter = 250 mm.

Mounting Instructions

Based on the previous section the following mounting instructions are recommended:
• A minimum distance X = 20 cm between gate unit and other converter parts like bus bars or clamp/ snubber circuits carrying high di/dt is necessary.
• The maximum magnetic field applied to the gate unit corresponds to the field of an aircore coil with 9 windings, diameter = 250 mm, peak current
40 kA and a distance X = 30 cm to the gate unit. However, EMI is an issue of the complete application set-up. We recommend carrying out qualification tests at converter level.

Thermal management

Due to the strongly load dependent power consumption, the recommended maximum ambient temperature is also a function of the load. Figure 20 shows the resulting operating diagram for lifetime operation of an IGCT device.
Continuous operation outside these limits will not cause immediate malfunction, but will reduce the lifetime of the on-board turn-off capacitors. The curve $P_{GIN\ Max}$ marks the limit of the power supply and must not be exceeded.
• Calculated lifetime of on-board capacitors 20 years.
• With slightly forced air-cooling (air velocity > 0.5 m/s).
• Strong air-cooling allows for increased ambient temperature.

Short-time operation slightly outside the recommended area in an overload situation may still be allowed if continuous operation has an acceptable margin to the limits. If operation outside the area recommended in figure 20 is required in steady state, improved air circulation will help to keep capacitor temperatures below acceptable limits.
Due to the poor predictability of the effect of equipment air circulation, it is advisable to measure gate unit capacitor temperature under worst-case converter continuous operating conditions as part of a type test program. This to verify operation within acceptable limits.

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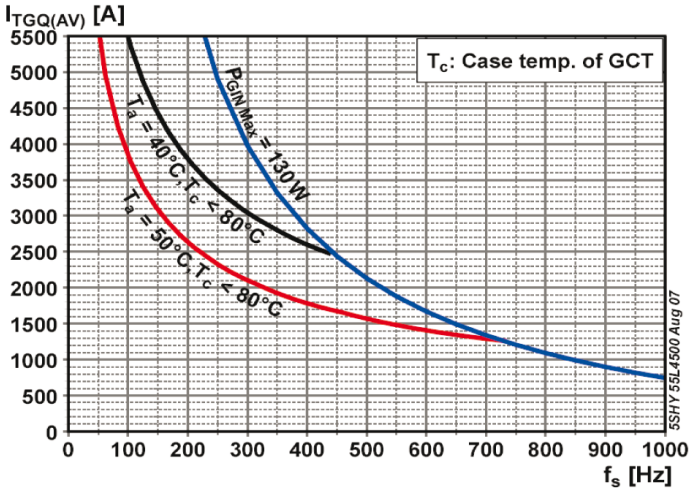


20 Maximum turn-off current for life time operation, example of an IGCT with a gate unit generation B

Vibration compliance

Vibration compliance is tested as follows: Industrial applications according IEC 68

- Endurance sine sweep 5 … 57 Hz +/-0.175 mm sine sweep 57 … 150 Hz 2.5gn
- Shock 15gn / 11 ms, 3 per direction, 30gn / 11 ms, 3 per direction

Packaged product, transportation

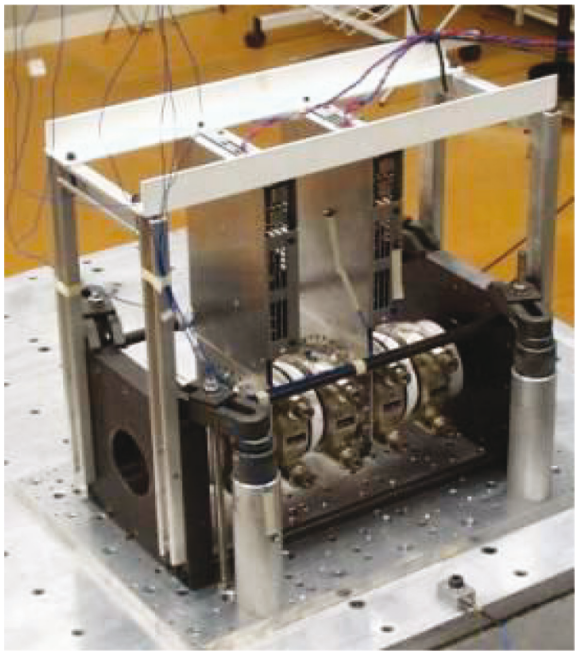
- Transport (IEC 721-3-2 Class 3)
- Shock (IEC 721-3-2 Class 3)
- Bump (IEC 68-2-29)

4. References

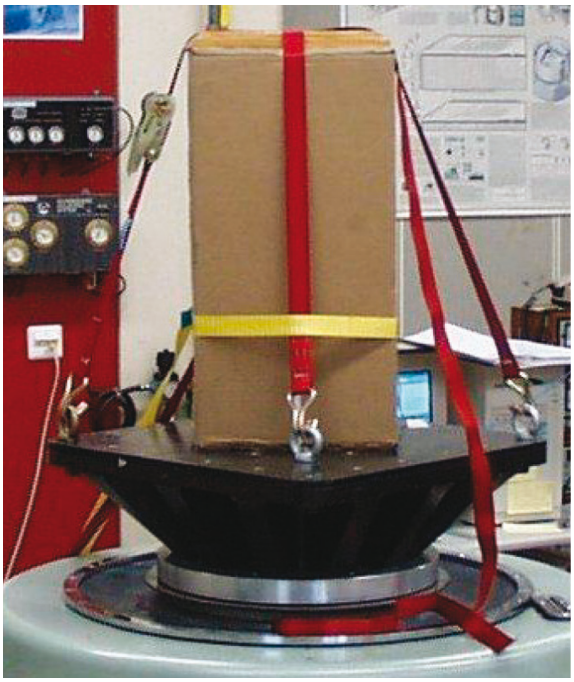
1) 5SZK9118 “General Environmental Conditions for High Power Semiconductors”
2) 5SYA2032 «Applying IGCTs»
3) 5SYA2036 «Recommendations regarding mechanical clamping of Press-pack High Power Semiconductors»
4) 5SYA2048 «Field measurements on High Power Press Pack Semiconductors»
5) 5SYA2051 «Voltage ratings of high power semiconductors»

5. Revision history

Version	Change	Authors
04		Thomas Setz Christoph Waltisberg
05	21.09.2015	Vasileios Kappatos Christoph Waltisberg
05	27.10.2017	Felix Mathis
06	09.12.2022	Christoph Waltisberg



21 Vibration test with IGCTs clamped in stack



22 Vibration test with IGCTs wrapped in transport box

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