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Application Note 5SYA 2034-02

Gate-drive recommendations for phase control and bi-directionally controlled thyristors

The main purpose of a gate-driver for a phase control thyristor (PCT) or a bi-directionally controlled thyristor (BCT) is to provide a gate current of the right amplitude, at the right time and of the right duration. This would seem simple, but the analysis of failures due to inadequate gate pulses shows that the proper design of a gate-drive unit is not trivial. This application note points out some of the most crucial gate-drive design rules.

1. Introduction

A thyristor is a current-controlled bipolar semiconductor, unlike MOSFETs or IGBTs which are voltage controlled. Therefore, a thyristor gate-drive unit is primarily a current source, supplying a specifically shaped current pulse from gate to cathode. The voltage drop along the gate-to-cathode path is a function of the gate current, the anode current and the internal impedance between gate and cathode. For this reason, thyristor manufacturers specify gate-current pulses rather than gate-voltage pulses.

2. Gate-drive recommendations and application aspects

2.1. Definitions

To explain the definitions of triggering-data for Hitachi Energy thyristors we use, as an example, the tabular triggering-data from the data sheet of the 5STB 18U6500 BCT with definitions according to international standard IEC 60747.”

Triggering

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Max. rated peak forward gate current	I_{FGM}				10	A
Peak rev. gate voltage	V_{RGM}				10	V
Gate power loss	V_G		See Fig. 1			W

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate trigger voltage	V_{GT}	T_{vj} = 25 °C			2.6	V
Gate trigger current	I_{GT}	T_{vj} = 25 °C			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \times V_{RM}$, T_{vj} = 125 °C	0.3			V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \times V_{RM}$, T_{vj} = 125 °C	10			mA

Table 1 Tabular trigger data for device 5STB 18U6500.
[1)] Maximum ratings are those values beyond which damage to the device may occur

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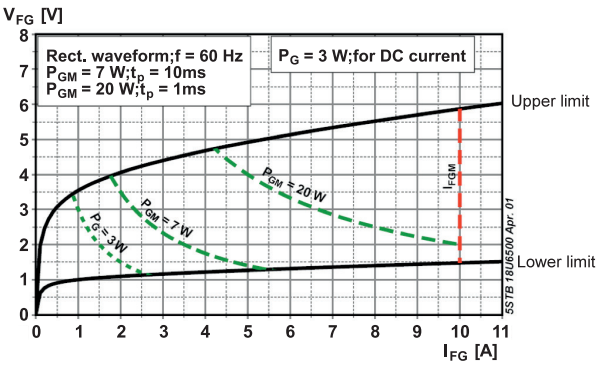
V_{FGM}: Maximum allowable forward gate-voltage. This voltage may instantaneously occur across the gate and cathode terminals if a strong initial gate pulse with a short rise-time and a high amplitude is applied and the anode current rises with a high di/dt.
I_{FGM}: This value indicates the maximum allowable gate-current, primarily determined by the gate contact. It is a maximum rating, valid for short pulses ≤ 100 microsecond (µs). For DC operation, I_{FGM} must be reduced further in order not to exceed the maximum continuous gate power-loss, P_G. Applying an I_{FGM} above the limiting value may be destructive due to over-stress of the internal gate-contact interfaces even if the average gate-power is within the specified limits.
V_{RGM}: Maximum reverse gate-voltage. Exceeding this rating will cause excessive reverse gate power-loss.
P_G: Gate power-loss. This is the maximum gate-power the thyristor can withstand without being damaged in the gate region. Values for typical conditions are presented in figure 1.
V_{GT}, I_{GT}: Gate trigger-voltage and current, respectively, defined as the minimum gate-voltage/current necessary to trigger the thyristor. These parameters are measured with an anode voltage of 6 volts (V) at a junction temperature of 25 °C. V_{GT} and I_{GT} decrease with increasing anode voltage and temperature. Note that these values are measured at quasi-stationary conditions. These values will just trigger the device and may lead to its destruction under worst-case conditions. Substantially higher values are needed in practice for operation under dynamic conditions, as will be explained later.
V_{GD}, I_{GD}: Gate non-trigger voltage and current, respectively, defined as the maximum admissible gate voltage/current which will not provoke triggering of the thyristor. These ratings are defined at quasi worst-case conditions of $V_D = 0.4 \cdot V_{DRM}$ and T_{vjmax} and will have higher values at reduced anode voltage and junction temperature. V_{GD} and I_{GD} are of particular importance in a noisy environment where electromagnetic interference can lead to spurious thyristor triggering. This may not only cause a malfunction of the converter but is also dangerous for the thyristor because marginal (localised) firing may destroy the gate structure. Special measures such as gate-signal filtering, should be implemented in these cases.
In addition to the tabular data, the data sheet also includes a gate characteristic curve, see figure 1.

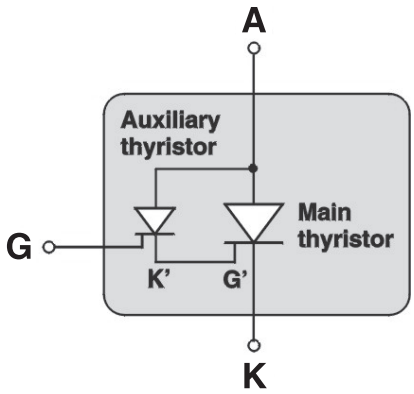


01 Gate characteristic curve from the 5STB 18U6500 data sheet

This curve shows the spread of V_{FG} as a function of I_{FG} considering both the effects of temperature, within the whole operational temperature range and whether the voltage is measured under static or dynamic conditions. The lower limit is the minimum expected DC gate voltage at T_j = -40 °C and the upper limit the highest expected dynamic gate-voltage at T_{vjmax}. The dotted hyperbolic lines show the instantaneous gate-power limits while the vertical dotted line represents the absolute gate-current limit of 10 ampere (A) which is not to be exceeded irrespective of duty cycle and pulse width.
The instantaneous gate-power limits are defined for three different pulse widths, where the pulse width t_p is either the width of a single rectangular pulse or the duration of a picket-fence pulse-train defined as time T in figure 9. For a single rectangular pulse, the load-line, see figure 7, must be drawn on the left side of the corresponding hyperbolic line for the appropriate pulse width. For a picket-fence pulse-train it must be assured that the gate current, the resulting gate voltage and the duty cycle, defined as the ratio T_{pn}/T_{rep} in figure 9, are selected to limit the rms-power to a value below the allowable P_{GM} of the chosen t_p.

2.2. Gate design and characteristics of Hitachi Energy thyristors

Small-area devices can be triggered properly by a relatively moderate current applied to a small gate region in the center of the device. For large-area devices of similar gate design, a substantial current would be required and it would also then take a relatively long time to get the whole device conducting. To avoid these problems, Hitachi Energy uses amplifying gates with interdigitation for large-area devices. The amplifying gate allows even the largest thyristors to be triggered with a low external gate-current. This is achieved by integrated gate-current amplification and allows the user to trigger all Hitachi Energy's PCTs and BCTs with the same gate-unit design. The amplifying gate consists of an auxiliary thyristor integrated in the main thyristor. This auxiliary thyristor is first triggered and supplies the required gate-trigger current for the main thyristor from the supply (anode) voltage. Schematics of the working principle and its implementation into the silicon wafer are shown in figures 2 and 3.



02 Basic principle of the amplifying gate

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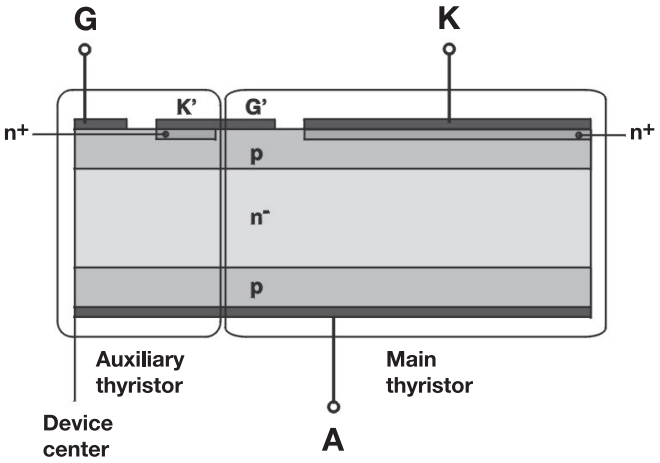
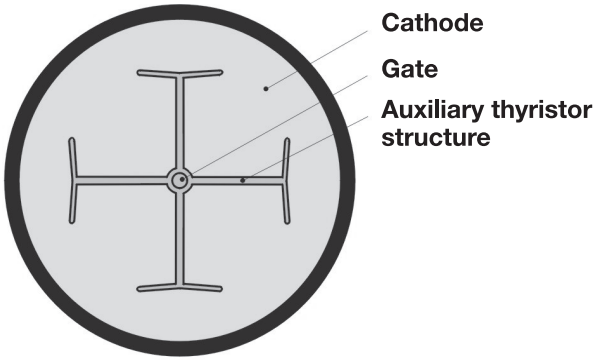
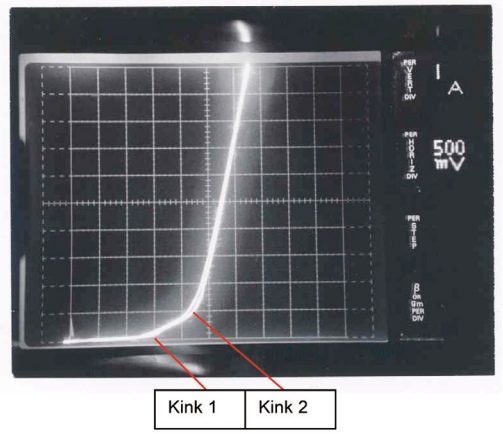


03 Lateral integration of the amplifying gate



04 View of thyristor wafer with distributed gate (T-Gate)

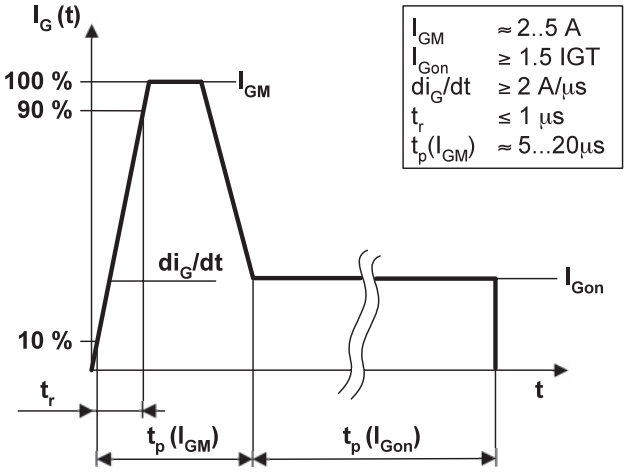
To further improve the turn-on behaviour of the device, the auxiliary thyristor structure may be distributed over the whole thyristor area, thus accelerating the spread of the conducting region during turn-on. This reduces turn-on losses and allows higher di/dt ratings as compared to simple central-gate structures. Hitachi Energy frequently use the T-gate design for the distributed auxiliary thyristor structure shown in figure 4.
The gate characteristics for a device with amplifying gate can be seen in figure 5. A repetitive AC gate current with peak value 10 A is applied and in figure 5, two «kinks» can easily be seen representing the triggering of the auxiliary and subsequently, the main thyristor.



05 Amplifying gate characteristic of thyristor 5STP 26N6500

2.3. Recommendations with regards to gate-current, gate-drive and load-line

Even though a thyristor can be triggered at static conditions by a current level of I_{GT}, a gate current with an amplitude of several times I_{GT} is needed for proper triggering achieving the desired performance at dynamic conditions. Based on the experience that Hitachi Energy has gathered over many years, we recommend a gate pulse as shown in figure 6.



06 Recommended gate-pulse for Hitachi Energy phase-control thyristors

The initial part of the gate pulse, characterised by the parameters I_{GM}, di_G/dt, t_r and $t_p(I_{GM})$, strongly affects the following thyristor characteristics and ratings:
- Turn-on delay time
- Turn-on fall time of the anode voltage
- Turn-on switching energy loss
- Critical di/dt of the anode current at turn-on.

A high I_{GM} and a low t_r, i.e. a high di_G/dt enhance all of these ratings and characteristics. The importance of these parameters in various applications is discussed in the following paragraphs. Although I_{GM} should not exceed 10 A, as indicated in the data sheet (I_{FGM} rating),

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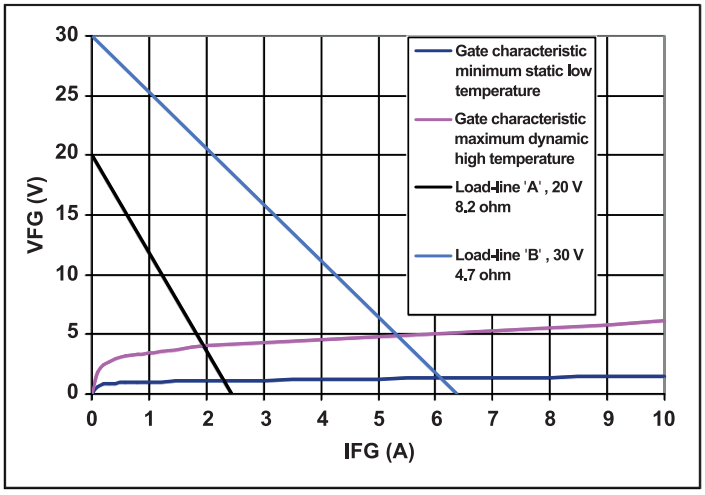
there is no upper rating limit for di_G/dt and is determined by the driving voltage, the gate-lead inductance and the gate-cathode voltage. The duration of the gate-current overshoot, $t_p(I_{GM})$, should be in the range specified on figure 6; 5 µs are sufficient for di/dt ≥ 20 A/µs but 20 µs would typically be required for di/dt ≤ 5 A/µs. For very low anode di/dt, the fall time for I_{GM} should not be too short since the device may turn off if the gate current drops too quickly. To achieve the recommended gate pulse and to avoid severe distortion of the gate current described in paragraph 2.8, the gate-driver should be designed with an appropriate load-line. By drawing the load-lines on the gate-characteristic graph, the resulting gate current can be determined. Some examples are included in figure 7.



07 Examples of gate-driver load-lines

Load-line «A», (20 V/8.2 Ω), resulting in a gate current of about 2 A at dynamic conditions can be considered «acceptable» for normal applications whereas Load-line «B», (30 V/4.7 Ω), resulting in a gate current of about 5.5 A at dynamic conditions, can be recommended for high di/dt applications and for applications with series- and/or parallel-connected thyristors.

2.4. Recommendations for crow-bar and other high di/dt applications

That the conduction area of the thyristor is initially quite small, it is not a problem for many line-commutated applications since the rate-of-rise of load current is moderate and matched by the rate-of-rise of conducting area. For other applications however, with either a high repetitive rate-of-rise of load current or with single pulses with high di/dt and high peak-current, the relatively slow rate-of-increase of conducting area represent a potential danger due to the initially high current density close to the gate region. Since this region has poorer cooling than the main volume of the device due to the gate contact, there is a risk of local over-heating leading to device failure. A strong initial gate-pulse will ensure that the amplifying gate and the main gate fire homogeneously allowing maximal device ratings to be achieved.

A weak gate-pulse may lead to localised gate-current and consequent local anode-current flow resulting in a «hot-spot» with subsequent device failure. It should be mentioned that pressure homogeneity is essential for full di/dt capability. For recommendations concerning design and verification of pressure homogeneity, please consult application note 5SYA 2036-Mechanical clamping of press-pack.

Another risk at very high di/dt, is the instantaneous potential difference between gate and cathode. This voltage comes from the lateral gate-current flow in the finger structure and can lead to flash-over between gate and cathode; it is a further limitation to high, non-repetitive di/dt performance. The di/dt capability can be increased somewhat by the use of a gate-driver with a sufficiently high driving voltage. For high di/dt applications such as those of «crow bars», the anode di/dt can initially be limited by the use of a saturable inductor. This allows the thyristor to expand the conduction area around the gate before the inductor saturates and the high di/dt appears.

2.5. RC-snubber and parasitic capacitance discharge

In many thyristor applications, anode current pulses with very high di/dt from the «snubber dump», discharge of parasitic cable capacitances and of other parallel capacitances, will occur. Parallel capacitances are sometimes used in systems with series-connected thyristors to ensure that all thyristors receive an initial high current peak to force the devices to turn on simultaneously. In some cases, current peaks come from voltage dividing capacitors. These are used to reduce the voltage stress on the converter in the case of fast surges from the supply line, since they form a voltage divider with the capacitances in the supplying transformer. In all these cases, the current rises very steeply, sometimes at several 100 A/µs or even at above 1000 A/µs when the thyristor triggers because the loop resistances and inductances can be quite small. Depending on device design, the maximum current peak allowed for such current pulses with very high di/dt, is 100 – 300 A, with some devices being able to handle up to 400 A. This rating is not specified in Hitachi Energy thyristor data sheets but is indirectly included since the rated di/dt is measured with an application-typical RC-circuit which provides an additional di/dt stress. The data sheet di/dt rating however defines only the main current rate-of-rise. The peak current from the discharge of this RC-circuit is normally in the range of 50 – 100 A and to this a small current from the stray capacitance in the measurement system is added. The influence of additional capacitance has for some devices been tested by parallel connection of discrete capacitors to simulate stray capacitance. One example from such a test is seen in figure 8. A gate pulse as recommended in figure 6 is in most cases suitable to handle these currents.

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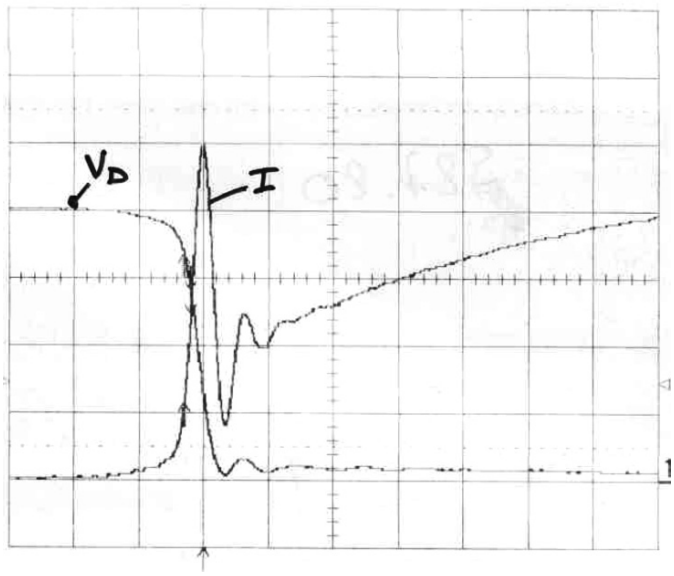
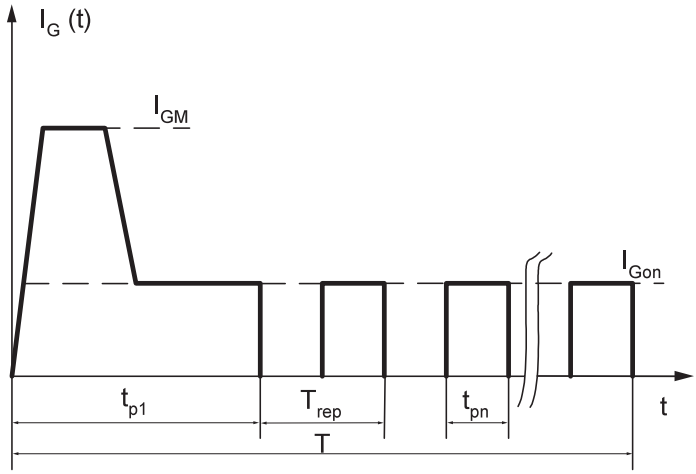


08 Discharge of 20 nF parasitic capacitance using 5STP 25L5200 at V_D = 4000 V, t = 0.5 µs/div, I = 100 A/div, T_j = 90 °C



09 Example of a picket-fence gate-pulse train

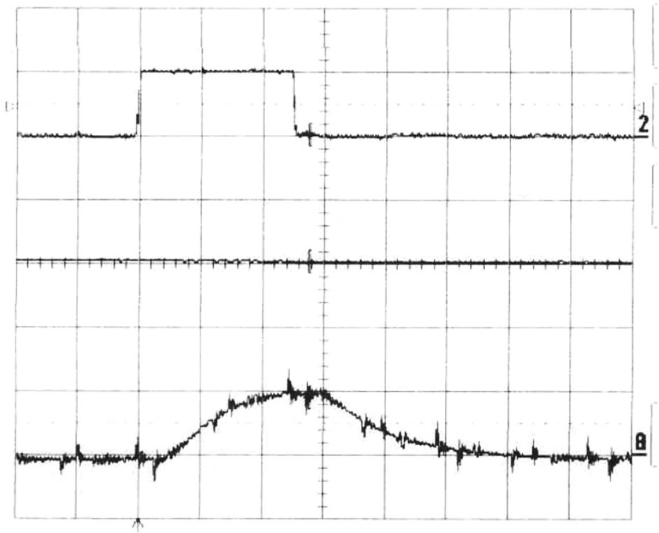
2.6. Back-porch currents and picket-fence current-pulses

«Back-porch current» (I_{Gon}) is required to keep the thyristor in the on-state when the anode current falls below the holding current IH, typically in «discontinuous-current mode» in controlled rectifiers or at line-voltage reversal. Ideally a thyristor is fired when forward biased but the gate-driver signal cannot always be synchronised with the load current. Back-porch current ensures that the thyristor will resume conduction when the anode voltage becomes positive again. Due to the lower current of the back-porch pulse, the di/dt capability at back-porch triggering is lower than when firing with a pulse shaped per figure 6. It is recommended to use a back-porch current, $I_{Gon} \geq 1.5 \cdot I_{GT}$ where I_{GT} is the maximum gate-trigger current at the minimum junction (or ambient) temperature. As stated in the next paragraph, care should be taken to minimise the time during which gate current is applied to the device in the reverse-blocking state, be it due to synchronisation problems or to long back-porch current-pulse durations. To reduce the power needed for the gate unit, I_{Gon} is often realised with «picket fence» current pulses as illustrated in figure 9.

The duration of the back-porch current must be sufficient to ensure that the thyristor is able to trigger at any time in the prospective conduction period, per the discussion above (I_{Gon}). It is recommended to have the first pulse t_{p1} longer than 30 µs and to have a duty cycle $t_{pn}/T_{rep} \geq 0.5$. Typical values for T_{rep} are 20 – 100 µs.

2.7. Gate current during reverse blocking

When the thyristor is in its reverse-blocking state, there is no risk of triggering neither by a positive nor by a negative gate-current. However, applying reverse anode-voltage and positive gate-current simultaneously will lead to an increased leakage current. A reverse-biased thyristor will act as a transistor with a gain in the range of 0.1 – 0.5. A gate current of 1 A can cause an increase in the leakage current of some hundreds of mAs even at room temperature. This leakage current can, in certain circumstances, lead to device failure and should be avoided. An example of the transistor action is seen in figure 10.



10 Leakage current increase due to gate current for 5STP 25L5200 at V_R = 1500 V, I_G = 2 A (channel 2), T_j = 100 °C, I_r = 200 mA/div (channel B), t = 20 µs/div

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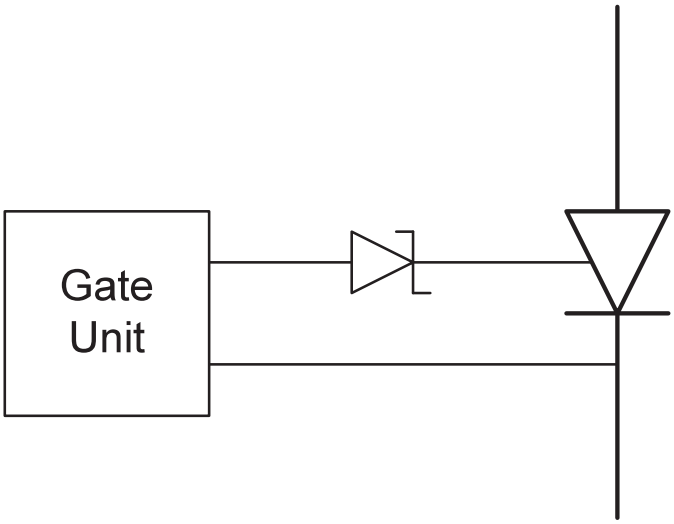
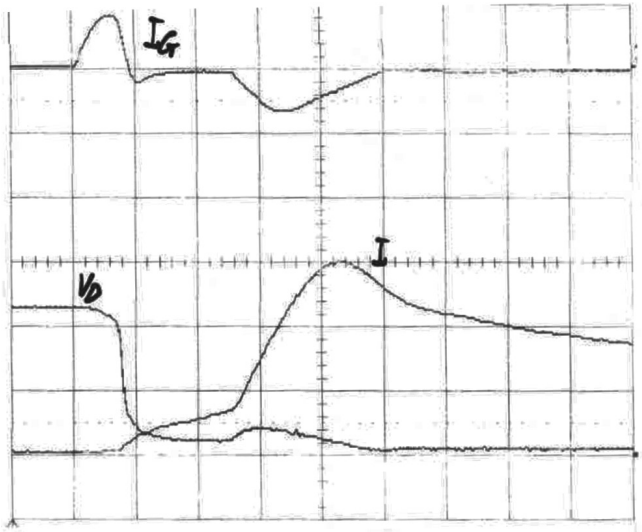


11 Simplified circuit diagram showing the insertion of a Schottky-Diode to protect the gate-driver



12 Gate current distortion at very high di/dt, t = 2 µs/div, I_G = 5 A/div, V_D = 2kV/div, I = 1 kA/div, thyristor 5STP 12N8500 at T = 90 °C

2.8. Gate current distortion

At the beginning of this application note, it was stated that the gate voltage reflects the reaction of the thyristor to the applied gate-current. In the first phase of the turn-on process, the gate-to-cathode impedance is higher than the steady-state value given in the data sheet (V_{FG} vs. I_{FG}). The dynamic gate-voltage is a function of the charge carrier concentration in the gate region, the internal inductances and the di/dt of the anode current. At high di/dt, the amplifying gate needs a high current to turn on the main thyristor. This current is provided by the auxiliary thyristor and it raises the gate voltage due to the impedance of the distributed gate structure.

With the recommended gate-pulse, the peak gate-voltage V_{GM} can reach amplitudes of 12 volts or more. This has to be considered when the voltage source for the gate-pulse amplifier and the gate-pulse transformer are designed. If the open-circuit gate-drive voltage is too low, the gate current may be considerably distorted; I_G (t) may have an instantaneous minimum close to zero or even become negative. Both cases can be dangerous for the thyristor and may lead to failure. This behaviour also needs to be considered when designing the thyristor gate-driver since it must be able to withstand a negative gate current without destruction. This is often accomplished by the use of a diode, preferably a Schottky-Diode, in series with the gate-driver as shown in figure 11.

In this context it is recommended that the design of the gate unit allow for gate-current measurements under worst-case conditions (max. anode di/dt), where possible. A gate-drive supply voltage of ≥ 20 V for moderate di/dt applications and ≥ 30 V for high di/dt requirements, is recommended. An example of pronounced gate-current distortion resulting from a gate-driver voltage lower than the dynamic gate-voltage, is shown in figure 12.

2.9. Triggering considerations for the serial and parallel connection of thyristors

Series-connected thyristors:

At turn-on, it is important that all individual devices switch simultaneously, otherwise the slower devices may be subjected to overvoltage. Besides the importance of simultaneous trigger-signals for all devices, differences in delay times, Δtd, in a stack of series-connected PCTs, must be minimised by the application of a strong gate-pulse which minimises the absolute value of td itself. Voltage imbalances at turn-on, which will always be present because of parametric scatter and different junction temperatures, are further reduced by an RC snubber-circuit across each device. The RC snubber is generally already present in most applications to limit voltage overshoot during reverse recovery.

Parallel-connected thyristors:

The imbalance in the turn-on characteristics of parallel connected thyristors is also minimised by a strong gate-pulse applied simultaneously to all devices. This is required for good current-sharing during the dynamic turn-on phase. Normally there is no need to select devices regarding td for adequate current sharing but in rare cases, it may be needed.

2.10. Spurious triggering due to electro-magnetic interference

Thyristors are operated in electrically noisy environments. In order to minimise the inductance of the gate lead and hence, the noise sensitivity, it is advantageous to mount the gate-driver as close as possible to the thyristor and to twist the gate leads or to use coaxial cables. Care must be taken that gate leads are not in contact with high voltage or high current parts in order to avoid electromagnetic

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interference or even flash-over to the gate leads. Sometimes a gate filter may be needed but then caution must be taken to ensure that the filter does not excessively attenuate the gate pulse.
To determine what short-duration (≈1.5 µs) noise levels can trigger a device, tests were performed on device 5STP 28L4200 at an anode voltage V_D = 200 V. The current levels needed to trigger the thyristors were:

at T_C = 25 °C, I_G = 495 - 655 mA with average value 590 mA.
at T_C = 50 °C, I_G = 460 - 560 mA with average value 517 mA.
at T_C = 80 °C, I_G = 390 - 530 mA with average value 472 mA.

3. Additional notes

3.1. Trigger signal transmission and power supply for the gate-drive unit

Since thyristors are at line potential and the control system, in most cases, is a low-voltage circuit at ground potential, the gate signal to the thyristor must be galvanically separated from the control system. There are several possibilities to accomplish this and the choice normally depends on the voltage level of the system. For low voltage systems, the gate current is transferred through a pulse transformer that provides the required isolation. For medium and high voltage systems, the gate pulse is often generated on a PCB at high potential. The common design is to send the gate pulse from the control unit through an optical fibre to the gate-driver which gets its power either from an insulated power supply or from the anode voltage. Another possibility is to send a high current pulse through a closed loop inductively coupled to the gate-driver providing power to the gate unit as well as triggering the gate units to emit synchronised gate pulses to the thyristors. This design is less prone to spurious triggering since the gate-driver is only energised when the current pulse is applied. It is important to design the gate-driver so that the main circuit does not influence the gate pulses via capacitive or inductive coupling caused by the presence of high dv/dt and di/dt. This is particularly important when several functionally independent thyristors are fired by the same driver board.

3.2. References

1) IEC 60747 “Semiconductor Devices”
2) 5SYA 2036 “Recommendation regarding mechanical clamping of press-pack high power semiconductors”, available at www.hitachienergy.com/semiconductors.

4. Revision history

Version	Change	Authors
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