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Semi-Full-Bridge Submodule for Modular Multilevel Converters

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***Abstract*—The energy variations in each arm of the modular multilevel converter comprises two components. The first component relates to the difference between the instantaneous input and output power of each phase-leg, and the second component relates to the energy which is moved back and forth between the two arms of the phase-leg. The latter component can be reduced or even eliminated if the peak-to-peak amplitude of the alternating voltage is greater than the pole-to-pole voltage of the dc link. This will, however, require submodules which can insert negative voltages. Therefore, a semi-full-bridge submodule which uses less semiconductors than the conventional full-bridge is proposed. Simulation results shows that by using the negative voltage-levels the capacitor voltage ripple can be reduced by up to 59%. Experimental results also shows that a 7-level voltage waveform can be generated using only one semi-full-bridge submodule with two capacitors per arm.**

***Index Terms* – Modular multievel converter, full-bridge submodules, modulation index, energy ripple**

I. Introduction

The modular multilevel converter (MMC) was first presented in 2003 in [1], [2]. It has shown to be a suitable topology for high-voltage high-power applications such as high-voltage direct current transmission [3], [4] and high-power motor drives [5]–[9]. Each phase-leg of the MMC consists of a number of series connected converter cells, termed submodules. These submodules can, for example, be half- or full-bridges equipped with dc-capacitors. In the case when full-bridge submodules are used, direct ac-ac conversion becomes possible which makes the MMC an interesting solution also for railway supplies [10], [11]. Full-bridge submodules can also be interesting for certain ac-dc applications where high modulation indices are required, such as in wind power applications [12]. Other uses for full-bridge submodules include fault-protection since they are able to mitigate fault-currents originating from dc-side short circuits. The full-bridge submodule will, however, increase both the cost and conduction losses of the converter since twice the number of conducting components are connected in series compared to the half-bridge. In order to alleviate this problem, the double-clamp submodule was proposed, which only increases the number of conducting elements by 25% [13], [14]. Such a submodule can, however, not actively insert any negative voltages and its use is therefore limited to fault protection. In this paper, it is shown that by replacing two of the diodes in the double-clamp-submodule with active switches the resulting submodule can act as a semi-full-bridge with two positive voltage levels and one negative voltage level. This will allow higher modulation indices at ac-dc conversion at a lower cost compared to full-bridge submodules. Consequently, as shown in [15], [16], the energy variations in the converter arms can be significantly reduced by increasing the modulation index to 1.41.

The outline of this paper is as follows. In Section II the basic operating principles of the MMC and various submodule types are presented. In Section III the proposed submodule implementation is introduced and its operating principles, semiconductor requirements, and conduction losses are discussed. The simulations and experimental results are presented in Section IV, and finally, some concluding remarks are given in Section V.

II. MMC Operating Principles

A schematic diagram of a three-phase modular multilevel converter is shown in Fig. 1. Each phase leg of the converter consists of two arms, one upper arm connected to the positive dc terminal, and one lower arm connected to the negative dc terminal. Each arm consists of N series-connected submodules and one arm inductor. The purpose of the arm inductors is to limit fault currents and parasitic components in the arm currents. The submodules are typically two- or three-level converters with dc capacitors as shown in Fig. 1.

The converter is controlled in such way that the net transfer of energy to each submodule is zero. In this way the stored energy in the submodule capacitors can be kept stable and the capacitor voltages remain close to their nominal values. Consequently, the capacitors act as voltage sources that can be inserted or bypassed in the chain of series connected submodules. By varying the number of inserted submodules in a sinusoidal manner, an alternating multilevel waveform is generated at the ac terminal.

The modulation index is defined as the ratio between the peak-to-peak value of the alternating voltage and the pole-to-pole voltage of the dc-link. Accordingly, the modulation index m is given by

$$m = \frac{2\hat{V}_s}{V_{\mathrm{dc}}}, \tag{1}$$

where $\hat{V}_s$ is the amplitude of the alternating voltage and V_{dc} is the pole-to-pole voltage of the dc-link. The voltages which should be inserted in the upper and lower arms can then be expressed as

$$v_u = \frac{1}{2}V_{\mathrm{dc}} - \frac{1}{2}m\hat{V}_{\mathrm{dc}}\cos(\omega_1 t) \tag{2a}$$

$$v_l = \frac{1}{2}V_{\mathrm{dc}} + \frac{1}{2}m\hat{V}_{\mathrm{dc}}\cos(\omega_1 t), \tag{2b}$$

where v_u and v_l are the inserted voltages in the upper and lower arms, respectively. It is observed that the sum of v_u and v_l is always constant and equals the dc-link voltage. It can also be observed that if the modulation index is greater than 1.0, the minimum voltage which should be inserted in each arm will be negative. If the submodules consist of half-bridges with dc-capacitors it will not be possible to insert negative voltages in the arms which means that the maximum possible modulation index is limited to 1.0 (or 1.15 if third-order harmonic injection is used). However, if full-bridge submodules are used, negative voltages can be inserted in the arms and the modulation index is then only limited by the voltage rating of the submodules. In the literature it has been concluded that this can be used for reducing the voltage ripple in the submodule capacitors [15], [16], or to maintain the amplitude of the alternating voltage when the dc-link voltage is reduced [12].

A significant drawback of the full-bridge submodule is that it uses twice the number of semiconductors compared to the half-bridge. Not only will this increase the cost of the converter, but it will also increase the conduction losses since the

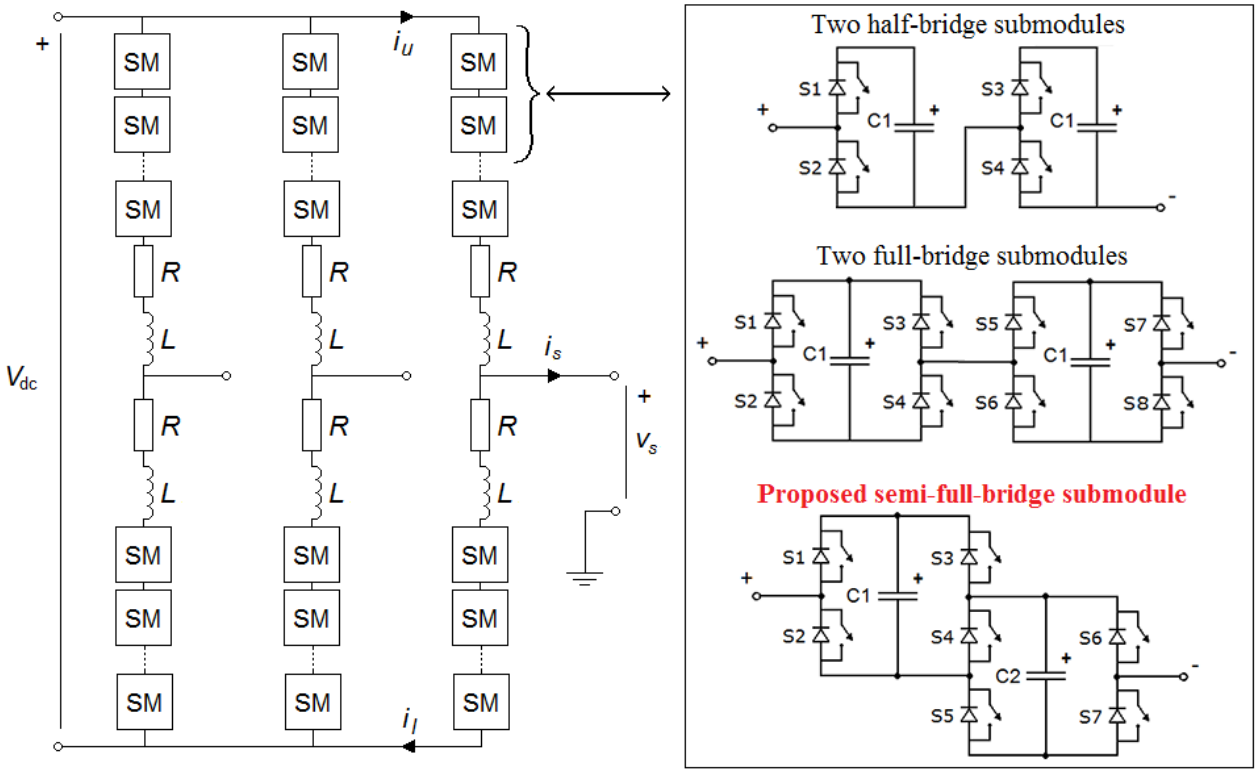

Fig. 1: Schematic diagram of a three-phase modular multilevel converter including the schematic diagrams of two half-bridge submodules, two full-bridge submodules, and the proposed semi-full-bridge submodule.

number of series-connected devices is doubled. Therefore, this paper proposes a submodule implementation that contains fewer semiconductors than the full-bridge, but still has the ability to insert negative voltages.

In order to ensure that the stored energy in the converter arms remains stable, the arm currents must contain both a direct and an alterating component at the fundamental frequency. That is,

$$i_u = \frac{1}{4}\hat{I}_s m\cos(\varphi) + \frac{1}{2}\hat{I}_s\cos(\omega_1 t - \varphi) \tag{3a}$$

$$i_l = \frac{1}{4}\hat{I}_s m\cos(\varphi) - \frac{1}{2}\hat{I}_s\cos(\omega_1 t - \varphi), \tag{3b}$$

where $\hat{I}_s$ is the phase-current, φ is the power angle, and i_u and i_l are the upper and lower arm currents, respectively. The directions of the currents i_u and i_l are defined as in Fig. 1.

A. Energy Variations

The instantaneous power input to each arm is given by the product of the arm voltage (2) and the arm current (3). Accordingly,

$$p_u = V_{\rm dc}\hat{I}_s\left[\frac{1}{2} - \frac{1}{2}m\cos(\omega_1 t)\right] \times \left[\frac{1}{4}m\cos(\varphi) + \frac{1}{2}\cos(\omega_1 t - \varphi)\right] \tag{4a}$$

$$p_l = V_{\rm dc}\hat{I}_s\left[\frac{1}{2} + \frac{1}{2}m\cos(\omega_1 t)\right] \times \left[\frac{1}{4}m\cos(\varphi) - \frac{1}{2}\cos(\omega_1 t - \varphi)\right], \tag{4b}$$

where p_u and p_l are the instantaneous power inputs to the upper and lower arms, respectively. Evaluating the product in (5) yields

$$p_u = V_{\rm dc}\hat{I}_s\left[-\frac{1}{8}m^2\cos(\varphi)\cos(\omega_1 t) + \frac{1}{4}\cos(\omega_1 t - \varphi) - \frac{1}{8}m\cos(2\omega_1 t - \varphi)\right] \tag{5a}$$

$$p_l = V_{\rm dc}\hat{I}_s\left[\frac{1}{8}m^2\cos(\varphi)\cos(\omega_1 t) - \frac{1}{4}\cos(\omega_1 t - \varphi) - \frac{1}{8}m\cos(2\omega_1 t - \varphi)\right]. \tag{5b}$$

It is observed that the direct components are canceled out. Consequently, the stored energy in the arms will not change over time. Instead, there will be a certain energy-ripple which must be handled by the submodule capacitors.

Integrating (5) and substituting $V_{\rm dc}$ with (1) yields

$$e_u = -\frac{\hat{V}_s\hat{I}_s}{2m\omega}\left[\frac{1}{4}m\sin(2\omega_1 t - \varphi) - \sin(\omega_1 t - \varphi) + \frac{m^2\cos(\varphi)}{2}\sin(\omega_1 t)\right] \tag{6a}$$

$$e_l = -\frac{\hat{V}_s\hat{I}_s}{2m\omega}\left[\frac{1}{4}m\sin(2\omega_1 t - \varphi) + \sin(\omega_1 t - \varphi) - \frac{m^2\cos(\varphi)}{2}\sin(\omega_1 t)\right], \tag{6b}$$

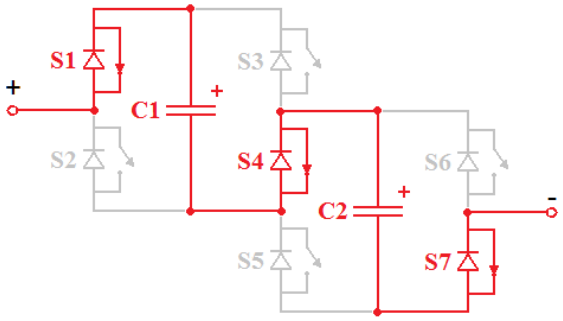

Fig. 2: Illustration of the switching states when the capacitors are inserted in series.

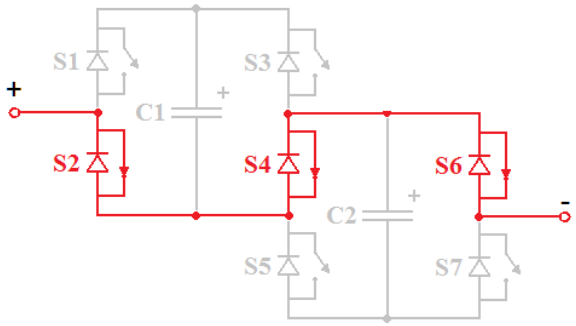

Fig. 3: Illustration of the switching states when the capacitors are bypassed.

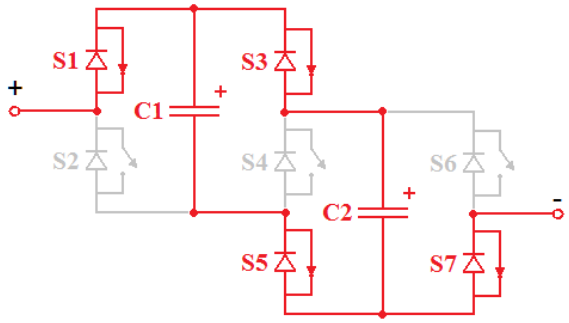

Fig. 4: Illustration of the switching states when the capacitors are inserted in parallel with a positive polarity.

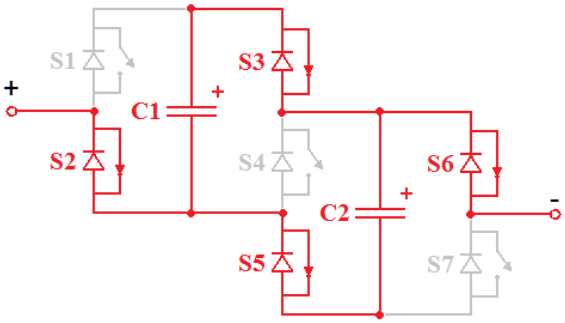

Fig. 5: Illustration of the switching states when the capacitors are inserted in parallel with a negative polarity.

where e_u and e_l are the alternating components in the stored energy in the upper and lower arms, respectively. It is observed that the energy-ripple in the arms consists of one common-mode component which is in phase in the upper and lower arms, and one differential-mode component which is in antiphase in the upper and lower arms. The common-mode component is an alternating component at twice the line-frequency and is a direct consequence of the fact that the active power at the dc-terminals is constant whereas the phase-power on the ac-side pulsates at twice the line-frequency. The differential-mode component, however, represents energy which is moved back and forth between the two arms. In [15], [16] it is shown that this component can be eliminated at active power transfer if the modulation index is increased to 1.4.

III. Semi-Full-Bridge Submodule

The negative voltage which should be inserted in case of modulation indices greater than unity is smaller than the maximum positive voltage which should be inserted. Therefore, a semi-full-bridge submodule which is able to insert two positive voltage leves but only one negative voltage level is proposed. The proposed semi-full-bridge submodule is shown in Fig. 1 and will hereafter be referred to as a SFB submodule. The SFB can be considered as an extension of the double-clamp-submodule presented in [13], [14]. The main difference between the double-clamp-submodule and the proposed SFB is that two diodes have been replaced by active switches which changes the function and operating principles of the submodule.

The proposed submodule contains two capacitors which can be bypassed, connected in parallel, or in series. This means that one SFB-submodule can replace two conventional half-bridge submodules. Therefore, when evaluating the SFB it must be compared to two series-connected half- or full-bridges as shown in Fig. 1. Although each SFB uses seven devices it is possible to control the SFB in such way that S_3 and S_5 are always conducting in parallel. This means that S_3 and S_5 must only be rated for half of the arm current. Thus, in terms of combined power rating of the semiconductors, the seven devices in the SFB corresponds to six devices rated for the full arm current. Accordingly, the combined power rating of the devices in the SFB is 50% higher compared to the half-bridge submodule, and 25% lower compared to the full-bridge submodule.

The relevant switching states of the SFB are illustrated in Figs. 2–5. In these illustrations, conducting on-state devices are depicted in red color, and devices that are turned off are shown in gray color. It is observed that the two capacitors are always connected either in parallel or in series. This means that if the capacitors C_1 and C_2 have the same capacitances, the voltages across C_1 and C_2 will always be equal. Consequently, in the ideal case there will not be any surge currents flowing between the capacitors when they are connected in parallel.

In Figs. 2–5 it can also be observed that for all switching states the current is conducted through three devices in series. If half-bridge submodules were used, only two devices would be connected in series per every two voltage levels, whereas four devices per every two voltage levels would be connected in series if full-bridge submodules were used. If the conduction losses in the diodes and the switches are considered equal this would mean that the conduction losses of the SFB are 50% higher compared to two half-bridges, but 25% lower when compared to two full-bridges.

The combined power rating of the devices, the number of conducting semiconductors in series, and the different features of the different submodule types are listed in Table I, where $\hat{V}_c$ is the peak capacitor-voltage, $\hat{I}_a$ is the peak arm-current, and V_c is the nominal capacitor voltage. It is observed that in most aspects the SFB is equivalent to the combination of one half-bridge and one full-bridge submodule.

TABLE I: Comparison of submodule circuits per every two positive voltage levels (as shown in Fig. 1).

	Half-bridges	Full-bridges	Proposed semi-full-bridge
Combined power rating of semiconductors	$4\hat{V}_c\hat{I}_a$	$8\hat{V}_c\hat{I}_a$	$6\hat{V}_c\hat{I}_a$
Available voltage levels	0, V_c, $2V_c$	$-2V_c$, $-V_c$, 0, V_c, $2V_c$	$-V_c$, 0, V_c, $2V_c$
Semiconductor devices connected in series	2	4	3
Modulation indices above unity	No	Yes	Yes
Blocking negative currents	No	Yes	Yes
Parallel connection of capacitors	No	No	Yes

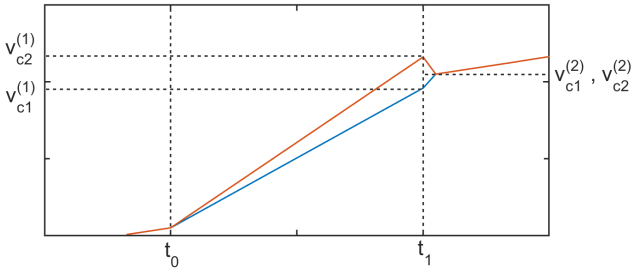

Fig. 6: Change in the capacitor voltages v_{c1} and v_{c2} when they are connected in series during the time-intervall $[t_0\ t_1]$.

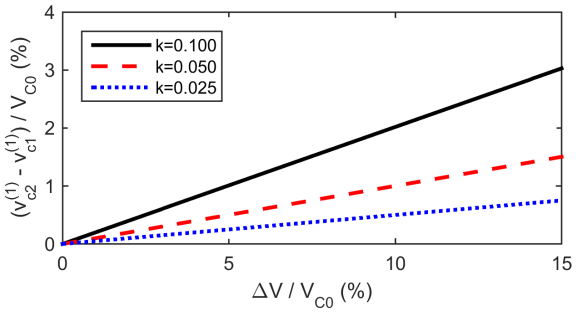

Fig. 7: Voltage difference between the capacitor voltages for different values of k as functions of ΔV. Both axes are shown in percent of the nominal capacitor voltage V_{c0}.

A. Voltage Balance between Capacitors

Ideally, the voltages across the two capacitors in each SFB would always be identical. In practice, however, the capacitor voltages will diverge when they are inserted in series since the capacitances of the two capacitors can never be exactly the same. This means that after the series connection of the capacitors, there will be a small difference between the two capacitor voltages. As a consequence, there will be a current spike and additional losses when the switching state is changed from series- to parallel-connection of the capacitors.

In order to evaluate the effect of a small difference in the capcitances, the capacitances C_1 and C_2 can be expressed as

$$C_1 = (1+k)C_0 \tag{7a}$$
$$C_2 = (1-k)C_0, \tag{7b}$$

where C_0 is the nominal capacitance and k indicates the maximum possible deviation in the capacitance values.

It is assumed that the capacitors are inserted in series at the time t_0, and then connected in parallel at the time t_1. The charge which is transferred to the capacitors during this time-interval is denoted q. The voltage across the capacitors at the time t_1 can then be expressed as

$$v_{c1}^{(1)} = V_0 + \frac{q}{(1+k)C_0} \tag{8a}$$
$$v_{c2}^{(1)} = V_0 + \frac{q}{(1-k)C_0}, \tag{8b}$$

where the superscript (1) is used to indicate that the equation describes the capacitor voltage at the time t_1 as shown in in Fig. 6. The voltage difference between the capacitors can then be expressed as

$$v_{c2}^{(1)} - v_{c1}^{(1)} = \frac{2k}{1-k^2}\Delta V, \tag{9}$$

where ΔV is given by

$$\Delta V = \frac{q}{C_0}. \tag{10}$$

As an example, consider the case when the capacitance of C_1 is 10% higher than the nominal value, and at the same time, the capacitance of C_2 is 10% lower than the nominal value. This corresponds to $k = 0.1$, and according to (9) the difference between the capacitor voltages will then be 20% of ΔV. This means that if ΔV is 5% of the nominal capacitor voltage, the difference in the capacitor voltages will be 1% of the nominal capacitor voltage. The differences in the capacitor voltages are shown in Fig. 7 in percent of the nominal capacitor voltage for different values of k as functions of ΔV.

B. Energy Losses due to Paralleling

From (9) it can be concluded that there will be a difference between $v_{c1}^{(1)}$ and $v_{c2}^{(1)}$ for all non-zero values of k. This means that when connecting the capacitors in parallel, there will be a current spike transferring a charge ϵ from capacitor C_2 to C_1 such that the two voltages becomes equal. The capacitor voltages can then be expressed as

$$v_{c1}^{(2)} = V_0 + \frac{q+\epsilon}{(1+k)C_0} \tag{11a}$$
$$v_{c2}^{(2)} = V_0 + \frac{q-\epsilon}{(1-k)C_0}, \tag{11b}$$

where the superscript (2) indicate the capacitor voltages after they have been connected in parallel. Setting (11a) equal to (11b) and solving for ϵ yields

$$\epsilon = kq. \tag{12}$$

Accordingly,

$$v_{c1}^{(2)} = V_0 + \frac{q}{C_0} \tag{13a}$$
$$v_{c2}^{(2)} = V_0 + \frac{q}{C_0}. \tag{13b}$$

Transferring the charge ϵ from C_2 to C_1 will cause additional losses. In order to evaluate these losses, the total energy which was transferred to the capacitors when they were connected in series is first calculated as

$$\begin{aligned} E_{\text{in}} = &\frac{1}{2}(1+k)C_0\left(v_{c1}^{(1)^2} - V_0^2\right) \\ &+ \frac{1}{2}(1-k)C_0\left(v_{c2}^{(1)^2} - V_0^2\right). \end{aligned} \tag{14}$$

Substituting (8) in (14) and simplifying the expression yields

$$E_{\text{in}} = \frac{2V_0 q C_0 (1-k^2) + q^2}{(1-k^2)C_0}. \tag{15}$$

The energy which is lost after the capacitors are connected in parallel can then be expressed as

$$\begin{aligned} E_{\text{loss}} =& \frac{1}{2}(1+k)C_0 \left({v_{c1}^{(1)}}^2 - {v_{c1}^{(2)}}^2 \right) \\ &+ \frac{1}{2}(1-k)C_0 \left({v_{c2}^{(1)}}^2 - {v_{c2}^{(2)}}^2 \right). \end{aligned} \tag{16}$$

Substituting (8) and (13) in (16) and simplifying the expression yields

$$E_{\text{loss}} = \frac{k^2 q^2}{(1-k^2)C_0}. \tag{17}$$

Accordingly, the relative losses can be expressed as

$$\frac{E_{\text{loss}}}{E_{\text{in}}} = \frac{k^2}{2V_0 \frac{C_0}{q}(1-k^2)+1}. \tag{18}$$

By substituting (10) in (18) and assuming $\Delta V \ll V_0$ the relative losses can be approximated as

$$\frac{E_{\text{loss}}}{E_{\text{in}}} \approx \frac{1}{2}\frac{k^2}{1-k^2}\frac{\Delta V}{V_0}. \tag{19}$$

As an example, a deviation of $\pm 10\%$ in the capacitor values and a 2% increase in the capacitor voltages during the time when they are connected in series results in 0.01% losses when the capacitors are connected in parallel.

The total energy losses in the submodules is related to the total amount of energy which is moved in or out from the submodule capacitors when they are connected in series. As a theoretical upper limit of the losses, the total energy-variations in the submodule capacitors can be considered. According to (6), at active power and the modulation index 1.0, the peak-to-peak energy variations in the arms are 4.1 kJ/MVA per arm. At 50 Hz this corresponds to 206.7 kJ per second, which is 20% of the transferred power per phase.

IV. Simulations and Experimental Results

A. Simulation Results

The functionality of the SFB is validated by simulating a converter with four SFB-modules per arm. In order to demonstrate how the negative voltage levels can reduce the capacitor voltage ripple the modulation index is first set to 1.0. The results are then compared with the case when the modulation index is increased to 1.4, which will require the negative voltage levels of the SFB-submodules to be used. In both simulations the power transfer is 9.6 MW per phase and the nominal energy storage in the capacitors is 25.0 kJ/MVA. The circulating current in the phase-leg is controlled so that it is a direct current. In the simulated system this is done by using a proportional control for the circulating current. The specifications of the simulated system are listed in Table II

1) Simulation with Modulation Index 1.0: When the modulation index equals 1.0, the dc-link voltage is set to 24 kV which means that the nominal capacitor voltage is 3 kV. The arm currents are shown in Fig. 8 and the inserted voltage in the lower arm is shown in Fig. 9. Since there are four SFB-submodules per arm, there are eight positive non-zero voltage levels in the arm voltage. The negative voltage spikes that can be observed in Fig. 9 appear as a consequence of the circulating current control.

The average capacitor voltages in the upper and lower arms are shown in Fig. 10. It is observed that there is a fundamental-frequency component in the capacitor voltages. This has a significant impact on the peak-to-peak value of the capacitor voltage ripple. In this case, the peak-to-peak value of the capacitor voltage ripple is 515 V, which corresponds to 17% of the nominal capacitor voltage.

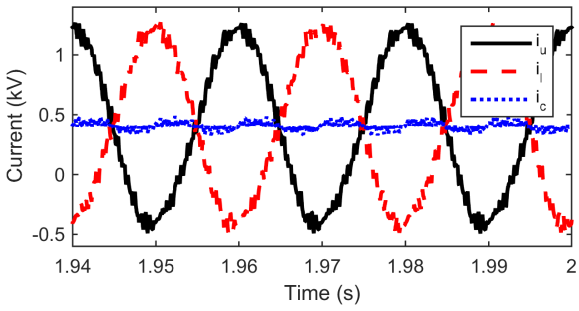

Fig. 8: Simulated arm currents (black solid, and red dashed), and circulating current (blue dotted), with the modulation index 1.0.

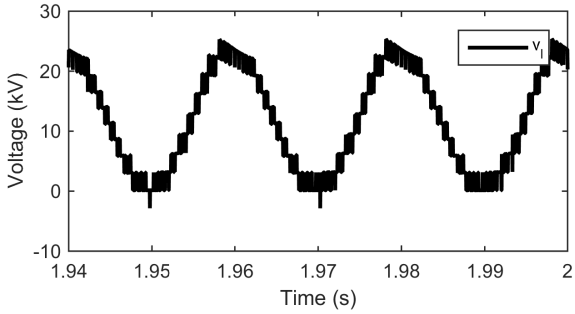

Fig. 9: Simulated arm voltage with the modulation index 1.0.

2) Simulation with Modulation Index 1.4: When the modulation index is set to 1.4, the dc-link voltage is reduced to 20 kV. In this way the nominal capacitor voltage will remain at 3.0 kV. The simulated arm currents are shown in Fig. 11. The direct current is slightly higher compared to the previous simulation owing to the reduced dc-link voltage. However, due to the increased modulation index, the amplitude of the alternating current is reduced and the peak-value of the arm current is therefore not increased. In fact, compared to the previous simulation the peak-value of the arm current is reduced from 1.27 kA to 1.23 kA.

The simulated arm voltage in the lower arm is shown in Fig. 12. Since the modulation index is greater than unity, negative voltage levels are used which results in two additional voltage levels in the alternating voltage. The main difference between the two simulations is, however, the capacitor voltage ripple shown in Fig. 13. It is observed that the fundamental-frequency component is almost fully eliminated. In fact, this

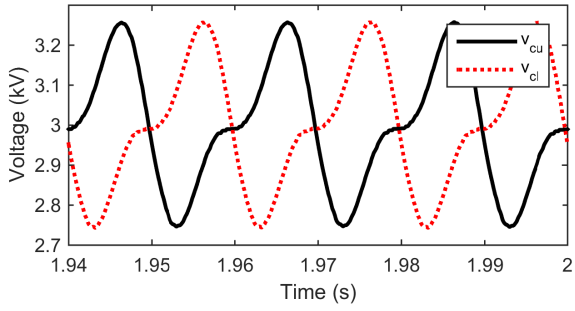

Fig. 10: Simulated capacitor voltages with the modulation index 1.0.

TABLE II: Simulation parameters.

	Simulation 1	Simulation 2
Power transfer	9.6 MW per phase	9.6 MW per phase
Phase voltage (rms)	8.27 kV	9.87 kV
Alternating current (rms)	1.16 kA	0.975 kA
Dc-link voltage	24 kV	20 kV
Number capacitors per arm	8	8
Nominal capacitor voltage	3.0 kV	3.0 kV
Arm inductance	1.38 mH (6%)	1.93 mH (6%)
Submodule capacitors	3.33 mF (25.0 kJ/MVA)	3.33 mF (25.0 kJ/MVA)
Modulation index	1.0	1.4
Peak-to-peak capacitor voltage ripple	515 V	210 V

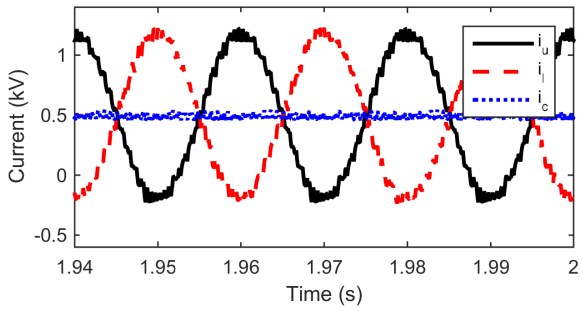

Fig. 11: Simulated arm currents (black solid, and red dashed), and circulating current (blue dotted), with the modulation index 1.4.

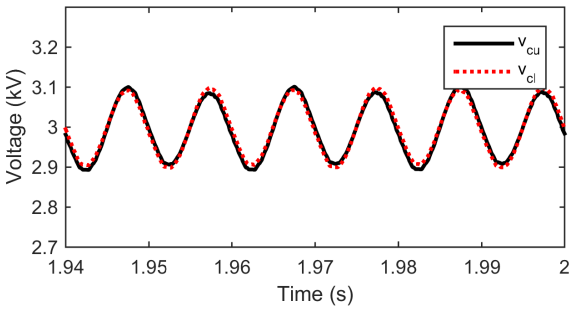

Fig. 13: Simulated capacitor voltages with the modulation index 1.4.

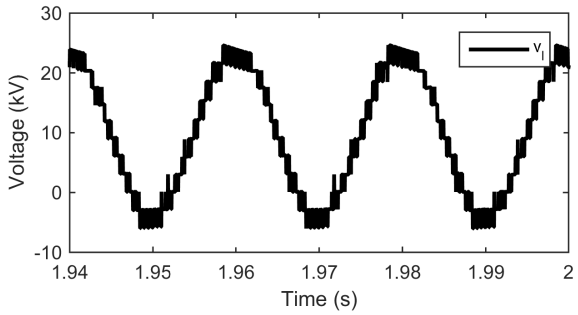

Fig. 12: Simulated arm voltage with the modulation index 1.4.

was expected since only active power is transferred and the modulation index is equal to 1.4 [15], [16]. As a consequence, there is a significant reduction in the capacitor voltage ripple. In fact, the peak-to-peak voltage ripple is reduced to 210 V, which corresponds to a 59% reduction compared to the case when the modulation index is 1.0.

B. Experimental Results

The proposed submodule implementation was validated experimentally in a single-phase configuration using one semi-full-bridge submodule with two 730 μF capacitors per arm. The dc-terminals of the setup are connected to a 100-V dc-supply and the ac-terminal is connected to a 40-Ω resistive load.

1) Implementation and Modulation: In order to utilize all available voltage levels of the SFB-submodules, the switching state of each submodule is determined using three phase-shifted carriers. In this way, a four-level waveform can be obtained as illustrated in Fig. 14. An offset is added to the reference waveform such that the zero-level corresponds to the case when the capacitors are connected in parallel with negative polarity, as shown in Fig. 14.

In order to obtain the maximum number of voltage levels at the ac-terminal, the same set of carriers are used to control both the upper and lower arm submodules. As a consequence, the first carrier harmonic that appears in the arm voltages will be canceled out at the ac terminal and $(2N+1)$-level modulation is obtained [17]. Since there are three non-zero voltage levels per arm this means that the epxerimental setup is expected to generate a seven-level voltage waveform. Furthermore, since there are three carriers per arm, the frequency of the first switching harmonics to appear in the arm voltages should be at three times the carrier frequency. However, since $(2N+1)$-level modulation is used, the first switching harmonics to appear at the ac-terminal are centered at six times the carrier frequency. In the experimental setup the carrier frequency is 325 Hz which means that the switching harmonics in the alternating waveform are expected to be centered at 1950 Hz.

2) Measurement Results: The measured output voltage and load current of the single phase setup are shown in Fig. 15 and Fig. 16, respectively. As expected, seven voltage-levels can be observed in the measured ouptut voltage. The harmonic amplitudes of the measured voltage are also shown in Fig. 17. As expected, the main harmonic content in the output voltage appear to be centered around 1950 Hz. The total harmonic distortion of the measured voltage is 15%, and the weighted THD [18], where the harmonics are weighted by 1 over the harmonic order n, is 0.8%.

V. Conclusions

This paper proposes a submodule implementation which allows two capacitors to be connected in parallel with both positive as well as negative polarity. The resulting negative voltage level can be used to increase the modulation index above unity, or simply to obtain a larger number of voltage levels using fewer capacitors. However, due to differences in the capacitance values there may be a small difference between the two capacitor voltages before they are connected in parallel. Although this may result in a current-spike when connecting the capacitors in parallel, the related energy-losses are very small. The proposed

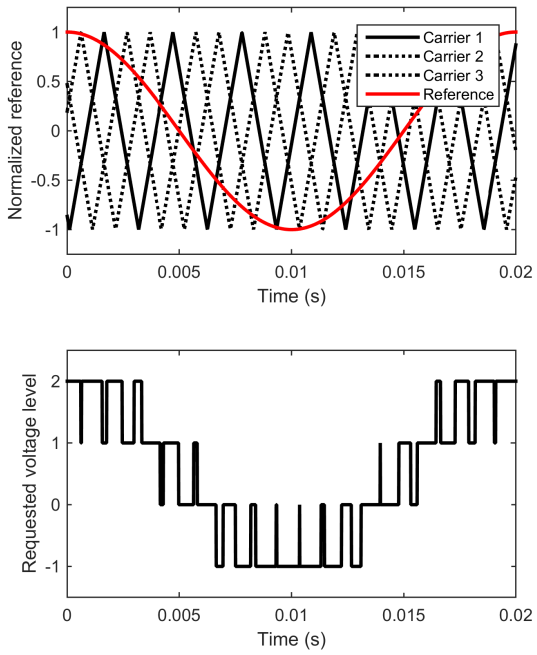

Fig. 14: Carrier waveforms (upper) and the corresponding voltage level (lower) of each SFB-submodule.

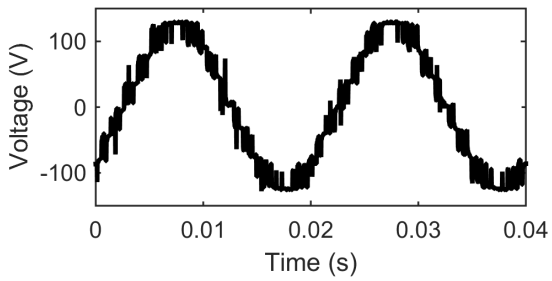

Fig. 15: Measured output voltage in the experimental setup.

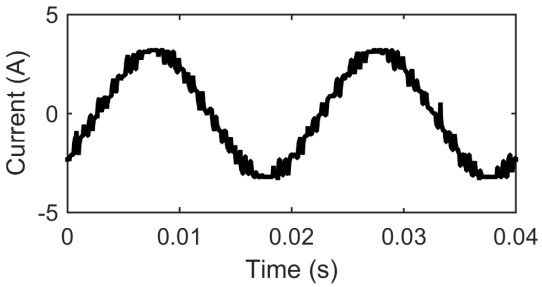

Fig. 16: Measured load current in the experimental setup.

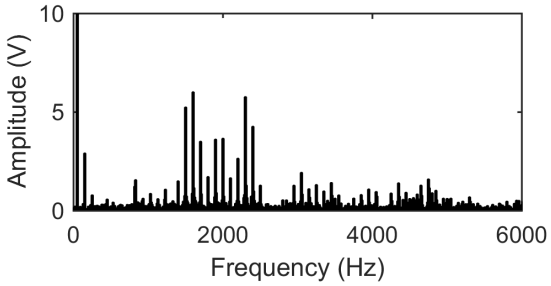

Fig. 17: Harmonic amplitudes of the measured output voltage in the experimental setup. The amplitude of the fundamental-frequency component is 124 V.

submodule was validated both by simulations and experimental results. It was concluded that the capacitor voltage ripple can be reduced by 59% compared to unity modulation index if the negative voltage levels are used. Successful operation of the proposed submodule was also demonstrated experimentally where a 7-level alternating voltage waveform was generated using only two capacitors per arm.

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