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Loss Evaluation for Modular Multilevel Converters with Different Switching Strategies

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***Abstract*—Apparently, modular multilevel converter (MMC) has been extensively used in high voltage direct current (HVDC) transmission links in recent years. The efficiency of MMC stations are highly related to the switching methods and semiconductor devices. So, various switching methods and semiconductor devices have been investigated and introduced in the field. This paper settles a benchmark for an HVDC link, based on a real project, and investigates the impact of six different switching methods on the converter loss, utilizing a commercial semiconductor device. The evaluation indicates that switching methods which consider the current level at switching instants are more efficient in comparison with the other methods which only consider the number of switching events. The result of this study is essential for more efficient converter stations.**

Keywords—Power conversion, HVDC transmission, Switching frequency, Switching loss.

I. Introduction

The use of high voltage direct current (HVDC) has emerged rapidly as a transmission technology in recent years and the modular multilevel converter (MMC) is one the most promising topologies for this technology [1]. High modularity, small footprint and lower losses are the prominent features of the MMC in comparison to previous topologies such as two-level converters [2]. Each phase of MMC is composed of series connected capacitors which are controlled by means of semiconductor devices. Phase voltages are instantaneously determined by capacitor voltage contribution of inserted cells. So, different phase voltage levels can be created by manipulating the switching signals for each converter cell. Consequently, the converter power losses are highly related to the switching methods and also the characteristic of the semiconductor devices in MMC [3]. Moreover, the converter footprint is influenced by the size of cell capacitor which, itself, is determined by the capacitor voltage ripple [4]. The switching method for MMC influences both cell capacitor voltages and also the semiconductor losses.

Many different switching methods are introduced and studied in literatures in order to reduce the MMC losses [5], [6] and/or to control the capacitor voltages [7], but these methods are investigated in different converter models with different operating conditions. So, it is difficult to identify the most efficient switching method with lowest converter losses. In order to overcome such a difficulty, a point-to-point HVDC link has been modeled as a benchmark in accordance to a real HVDC link and six different switching methods are investigated in order to find the most efficient one. All selected methods are based on tolerance band concept which are introduced in [6] and practically tested in real-time digital simulation environment.

In order to define a generic benchmark, a detail of loss calculation formulas has been presented in Section II-B. These formulas are modified to be used in time-domain simulation environment for conduction and switching loss calculations. Later in Section III, the selected methods are introduced and referenced. Section IV is devoted to the benchmark modeling and results discussion. The conclusion is drawn in Section V.

II. MMC Topology and Power Losses

The circuit configuration of the modular multilevel converter is illustrated in Fig. 1. Each phase consists of two arms, the positive and negative, which are connected from the positive and negative dc poles to the ac terminal, respectively. Each arm is formed by a series connection of N identical cells, and arm inductors L_{arm}. The basic cell topology is a half-bridge topology which is labeled in Fig. 1 as "single cell structure". It contains a dc capacitor C and two insulated gate bipolar transistors (IGBTs) Sw_{n1} and Sw_{n2}. Each cell has two possible switching states which select the corresponding terminal voltages to be equal to zero or v_{cap_n}.

A. Basic Operating Principles

Refereing to Fig. 1, the positive and negative arm currents ($i_p(i)$ and $i_n(i)$) can be presented as

$$i_p(i) = \frac{i_s(i)}{2} - \frac{I_d}{3}\,, \quad i_n(i) = -\frac{i_s(i)}{2} - \frac{I_d}{3} \tag{1}$$

where $i_s(i)$ and I_d are converter phase and dc current, respectively. Note that (i) denotes the arbitrary number of each phase.

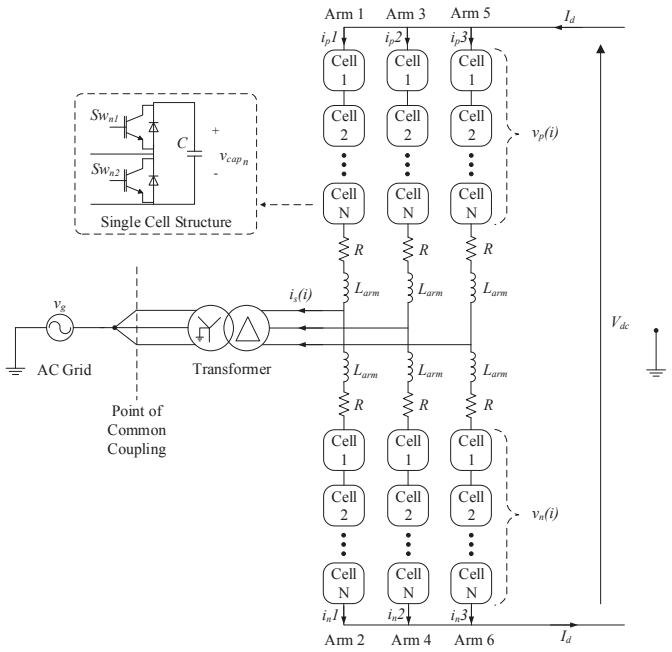

Fig. 1. Modular multilevel converter (MMC) topology

Then, the converter phase current ($i_s(i)$) is obtained from (1) as

$$i_p(i) - i_n(i) = i_s(i) = \sqrt{2} I_s(i) \cos(\omega t + \delta_s(i) - \varphi(i)) \quad (2)$$

where $I_s(i)$ is the phase current RMS value, $\delta_s(i)$ is the phase voltage angle and $\varphi(i)$ is the load angle. Substituting (2) in (1) yields

$$i_p(i) = \frac{\sqrt{2} I_s(i) \cos(\omega t + \delta_s(i) - \varphi(i))}{2} - \frac{I_d}{3} \quad (3)$$

$$i_n(i) = -\frac{\sqrt{2} I_s(i) \cos(\omega t + \delta_s(i) - \varphi(i))}{2} - \frac{I_d}{3}. \quad (4)$$

In addition, assuming an equal ac and dc side power, the dc current I_d can be represented as a function of converter power (P_c) and dc voltage (V_{dc}) as

$$I_d = -\frac{P_c}{V_{dc}} = -\frac{3 V_s(i) I_s(i) \cos\varphi}{V_{dc}} \quad (5)$$

where $V_s(i)$ and $I_s(i)$ are the phase voltage and current RMS value in i^{th} phase. Here the modulation index $m(i)$ is defined as

$$m(i) = \frac{2\sqrt{2} V_s(i)}{V_{dc}}. \quad (6)$$

Substituting (6) in (5) yields

$$I_d = -\frac{3 m(i) I_s(i) \cos\varphi}{2\sqrt{2}}. \quad (7)$$

So, the positive and negative arm currents can be presented as

$$i_p(i) = \frac{\sqrt{2} I_s(i) \cos(\omega t + \delta_s(i) - \varphi(i))}{2} + \frac{m(i) I_s(i) \cos\varphi}{2\sqrt{2}} \quad (8)$$

$$i_n(i) = -\frac{\sqrt{2} I_s(i) \cos(\omega t + \delta_s(i) - \varphi(i))}{2} + \frac{m(i) I_s(i) \cos\varphi}{2\sqrt{2}}. \quad (9)$$

The total number of cells in each arm is given by $N = \frac{V_d}{V_{cap}^{nom}}$ where V_{cap}^{nom} is the nominal converter cell capacitor voltage. Considering a positive arm in an arbitrary phase as an example, the number of inserted and bypassed cells ($n_p^{in}(i)$ and $n_p^{by}(i)$) can be calculated as

$$n_p^{in}(i) = \frac{\frac{V_{dc}}{2} - v_s(i)}{V_{cap}^{nom}} \quad (10)$$

$$n_p^{by}(i) = N - n_p^{in}(i), \quad (11)$$

by applying the Kirchhoff's voltage law and neglecting the voltage drop over arm inductor, L_{arm}. Substituting the sinusoidal representation of $v_s(i) = \sqrt{2} V_s(i) \cos(\omega t + \delta_s(i))$ and (6) into (10), the number of inserted and bypassed cells for that positive arm are given as

$$n_p^{in}(i) = \frac{N}{2}(1 - m(i) \cos(\omega t + \delta_s(i))) \quad (12)$$

$$n_p^{by}(i) = \frac{N}{2}(1 + m(i) \cos(\omega t + \delta_s(i))). \quad (13)$$

Since the dc-side voltage can be expressed by the summation of the positive and negative arm output terminal voltages of N number of cells, the negative arm insertion and bypass number ($n_n^{in}(i)$ and $n_n^{by}(i)$) is obtained by

$$n_n^{in}(i) = \frac{N}{2}(1 + m(i) \cos(\omega t + \delta_s(i))) \quad (14)$$

$$n_n^{by}(i) = \frac{N}{2}(1 - m(i) \cos(\omega t + \delta_s(i))). \quad (15)$$

Consequently, desired voltages and currents at the ac and dc terminals of MMC can be synthesized by controlling the number of inserted and bypassed cells in each converter arm. A proper switching technique can control the MMC in different operating modes and fulfill the system requirements.

B. Semiconductor Power Losses

The semiconductor loss is analyzed by considering mainly conduction loss and switching loss in this paper. However, the total converter loss includes other sources such as gate drive units, transformers and reactors which are not evaluated in this paper. For a half-bridge MMC cell, the semiconductor losses are divided into four parts, the upper-leg IGBT (T1) and diode (D1) losses, and the lower-leg IGBT (T2) and diode (D2) losses. The on and off states or cell operating modes depend on the directions of converter arm currents (positive arm i_p or negative arm i_n) flowing through the MMC cells. Taking the positive arm for instance, Fig. 2 shows the four MMC converter cell operating modes. The same mode analysis applies to the negative arm as well. The discrete integration

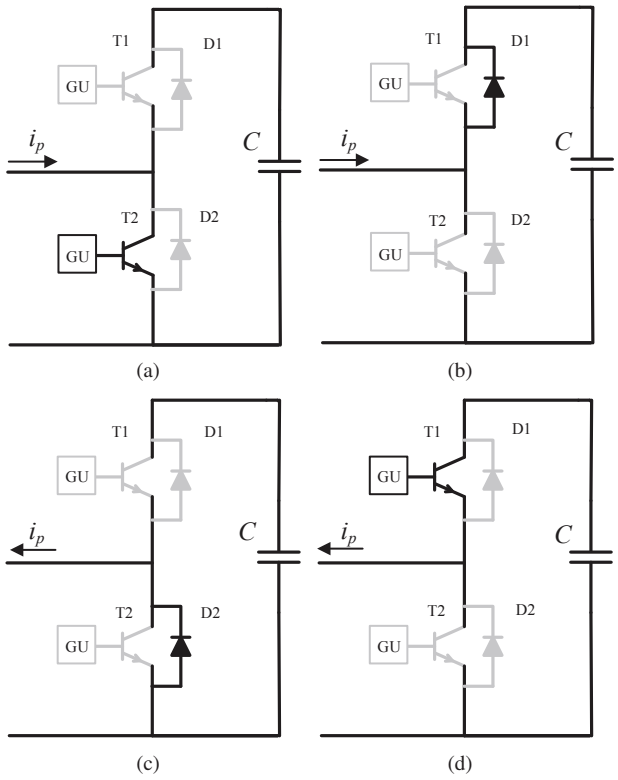

Fig. 2. Half-bridge cell operating modes (a) bypass ($i_p > 0$), (b) insert ($i_p > 0$), (c) bypass ($i_p < 0$), (d) insert ($i_p < 0$).

method and digital filtering are utilized in order to enable the time-domain calculation of power losses. The conduction and switching losses are calculated for each individual cell during the simulation run-time. The total converter losses are then determined by summing up the conduction and switching losses of all converter cells. The discrete calculation formulas for conduction and switching losses are presented as follow:

1) Conduction losses: The cell individual conduction loss is calculated based on the operating mode of the corresponding cell at each time step. Each cell can operate in any modes of Fig. 2. The IGBT and Diode conduction loss is calculated based on the conducting current and on-state resistance of the device in each time step. For instance the IGBT and Diode conduction loss of a cell in an arbitrary positive arm can be calculated as

$$\begin{aligned}
P^{in}_{D,cond}(t) &= (1-k)P^{in}_{D,cond}(t-1)+k(V_{F0}+R_D i_p(t))i_p(t)\\
P^{in}_{V,cond}(t) &= (1-k)P^{in}_{V,cond}(t-1)+k(V_{CE0}+R_{CE} i_p(t))i_p(t)\\
P^{by}_{D,cond}(t) &= (1-k)P^{by}_{D,cond}(t-1)+k(V_{F0}+R_D i_p(t))i_p(t)\\
P^{by}_{V,cond}(t) &= (1-k)P^{by}_{V,cond}(t-1)+k(V_{CE0}+R_{CE} i_p(t))i_p(t)
\end{aligned} \tag{16}$$

where

$P^{in}_{D,cond}$	is Diode conduction loss in D_1,
$P^{in}_{V,cond}$	is IGBT conduction loss in T_1,
$P^{by}_{D,cond}$	is Diode conduction loss in D_2,
$P^{by}_{V,cond}$	is IGBT conduction loss in T_2,
$i_p(t)$	is arm current at t instant,
V_{F0}	is Diode threshold voltage,
R_D	is Diode on-state resistor,
V_{CE0}	is IGBT threshold voltage,
R_{CE}	is IGBT on-state resistor and
$k = \frac{\Delta t}{T_{filter}}$	is filter constant.

Note that Δt and T_{filter} are simulation time step and filter time constant, respectively.

2) Switching losses: The energy dissipation at each switching event is proportional to the current level and the junction temperature at that instant. The maximum junction temperature of 125°C is assumed for both conduction and switching loss calculation. So, the switching power loss is extracted from the device data-sheet for each current level at each switching instants. The switching loss calculation can be implemented in time-domain study utilizing the following formulas:

$$\begin{aligned}
P^{in}_{D,sw}(t) &= (1-k)P^{in}_{D,sw}(t-1) + kE_{on,D}\big(i_p(t)\big)\\
P^{in}_{V,sw}(t) &= (1-k)P^{in}_{V,sw}(t-1) + kE_{on,V}\big(i_p(t)\big)\\
P^{by}_{D,sw}(t) &= (1-k)P^{by}_{D,sw}(t-1) + kE_{off,D}\big(i_p(t)\big)\\
P^{by}_{V,sw}(t) &= (1-k)P^{by}_{V,sw}(t-1) + kE_{off,V}\big(i_p(t)\big).
\end{aligned} \tag{17}$$

Where

$P^{in}_{D,sw}$	is Diode turn on power loss,
$P^{in}_{V,sw}$	is IGBT turn on power loss,
$P^{by}_{D,sw}$	is Diode turn off power loss,
$P^{by}_{V,sw}$	is IGBT turn off power loss,
$E_{on,D}\big(i_p(t)\big)$	is Diode turn on energy loss at $i_p(t)$,
$E_{on,V}\big(i_p(t)\big)$	is IGBT turn on energy loss at $i_p(t)$,
$E_{off,D}\big(i_p(t)\big)$	is Diode turn off energy loss at $i_p(t)$,
$E_{off,V}\big(i_p(t)\big)$	is IGBT turn off energy loss at $i_p(t)$ and
$k = \frac{\Delta t}{T_{filter}}$	is filter constant.

III. Switching Methods

(12) and (14) describe the ultimate control action of the MMC cells in each arm. The insertion index signal is continuously computed by the converter high-level control based on the converter operating point. However, the status of each cell is then determined through a cell selection method. Cell selection methods are to balance the cell voltage distribution and also to follow the computed reference insertion index. Six different switching methods are studied in this paper which are introduced in this section. All selected methods are either practically used in industries or already tested in real time simulators.

A. Phase-shifted pulse width modulation (PSPWM)

PSPWM has been introduced in [7] for modular multilevel converters. The method is widely used in different industrial applications. The method is based on conventional pulse width modulation method where the intersection between reference waveform and carrier waveform determines the switching

instants. This method assigns an specific triangular carrier waveform to each individual cell, while each carrier is phase shifted by $2\pi/N$ in which N is the number of cells per arm. Additionally, the generated arm reference is distributed among all cells in one arm. The individual cell switching pulse is generated locally at cell level. The switching frequency is determined by carrier frequency and consequently is similar for all cells. As is investigated in [3], there is a minimum limit on the carrier frequency and generally this method is not suitable for low switching frequency applications. As a reference, the carrier frequency of 200Hz is used in this paper which ends up to the 10% capacitor voltage ripple, average to peak.

B. Phase-shifted pulse width modulation + Sorting balancing (de-PSPWM)

Some references [3] have proposed to apply the sorting method on the phase-shifted PWM, in order to reduce the switching frequency and achieve better voltage balancing between cells. In this method, switching instants are determined by carrier, reference intersection but the switching cell is selected from the sorted list, literally, the modulation strategy is decoupled from the cell selection. Generally, the cells with low capacitor voltages and high capacitor voltages are prioritized for insertion in positive arm current intervals and negative arm current intervals, respectively. This method requires a central control unit to examine all capacitor voltages and select the proper cells.

C. Cell tolerance band + Sorting balancing (CTBsort)

As is proposed in [6], the cell capacitor voltages can tolerate a certain voltage ripple while charging and discharging. So, a fixed tolerance band can be utilized to determine the balancing action instants. Fig.3(a) illustrates the basic of this method. The required number of cells are selected from a sorted list of cell voltages which is updated at the time that any cell voltages hit the fixed tolerance band. In this way, the switching frequency can be reduced significantly, while the cell capacitor voltages are directly controlled by the fixed tolerance band.

D. Average tolerance band + Sorting balancing (ATBsort)

Similar to *CTBsort*, this method utilizes a tolerance band but over the cell average voltage in each arm. In this method, the sorted list is updated whenever a cell capacitor voltage excesses the defined tolerance band over the cell average voltage [6]. The detailed flowchart of this method is available in Fig.3(b). In comparison to *CTBsort*, this method increases the converter switching frequency but keeps the cell voltages more balanced.

E. Cell tolerance band + Sequential shifting (CTBsequence)

Rather than sorting method, the sequential shifting method requires no ranking action out of the cell voltages [5], [6]. The voltage balancing is achieved by reversing the cell assignment order in each cycle. However, the cell capacitor voltages are monitored against a fixed tolerance band which is set over the cell capacitor voltages. Fig.3(c) shows the principle flowchart of the method.

F. Optimized cell tolerance band method (CTBoptimised)

The optimized version of *CTBsort* is introduced in [8]. The method utilizes the current level at switching time to minimise the switching actions during the high current intervals and also to switch the cells for balancing purposes at zero current level. Utilizing this method charges the cells, with high capacitor voltages, up to the maximum cell voltage limit during the low current intervals while it reserves the cells with low capacitor voltages for high peak current intervals. The detail flowchart of the method is available in Fig. 3(d).

IV. Simulation Study

A. Benchmark setup

A point-to-point HVDC transmission link has been modeled as a benchmark setup in a time domain simulation tool, PSCAD™/EMTDC™. This setup is used to study different switching methods which are introduced in Section III, utilizing the Infineon 4.5kV IGBT device [9]. The benchmark converter rating is selected according to the real 2000MW point-to-point HVDC interconnection between France and Spain [10]. Fig. 4 illustrates the benchmark setup. Both MMC1 and MMC2 has the same topology as shown in Fig. 1. The system parameters for each station are shown in Table I. The control of each station is accomplished by separating the main current controller loop from the modulation and cell selection part. The reference voltages are generated through a generic open-loop controller which has been implemented according to [11] for each converter station. The generated reference voltages contain a fraction of 3^{rd} order harmonic (zero-sequence) in order to expand the voltage capability of the converter. The modulation and cell selection algorithms are implemented as discussed in Section III. In order to have a generic benchmark for different cell numbers, the total converter capacitor size is expressed in the form of energy density for rated power. On the other hand, a fixed strong network of 400kV with short circuit ratio equal to 10GVA is used in this study which can be considered a benchmark for different methods. The ac grid has a significant influence on the harmonic content at converter point of common coupling.

TABLE I. Circuit Parameters

Quantity	Notation	Value
Number of cells/arm	N	40
Rated active power	P	1 GW
Rated reactive power	Q	300 MVAR
Direct voltage	v_{dc}	320 kV
Alternating voltage	V	400 kV
Short circuit capability	SC	10 GVA
Rated frequency	f	50 Hz
Converter energy density	C	35 kJ/MW
Specified modulation index	M	0.8
Transformer leakage reactance	L_T	15%p.u.
Transformer Resistance	L_R	0.5%p.u.

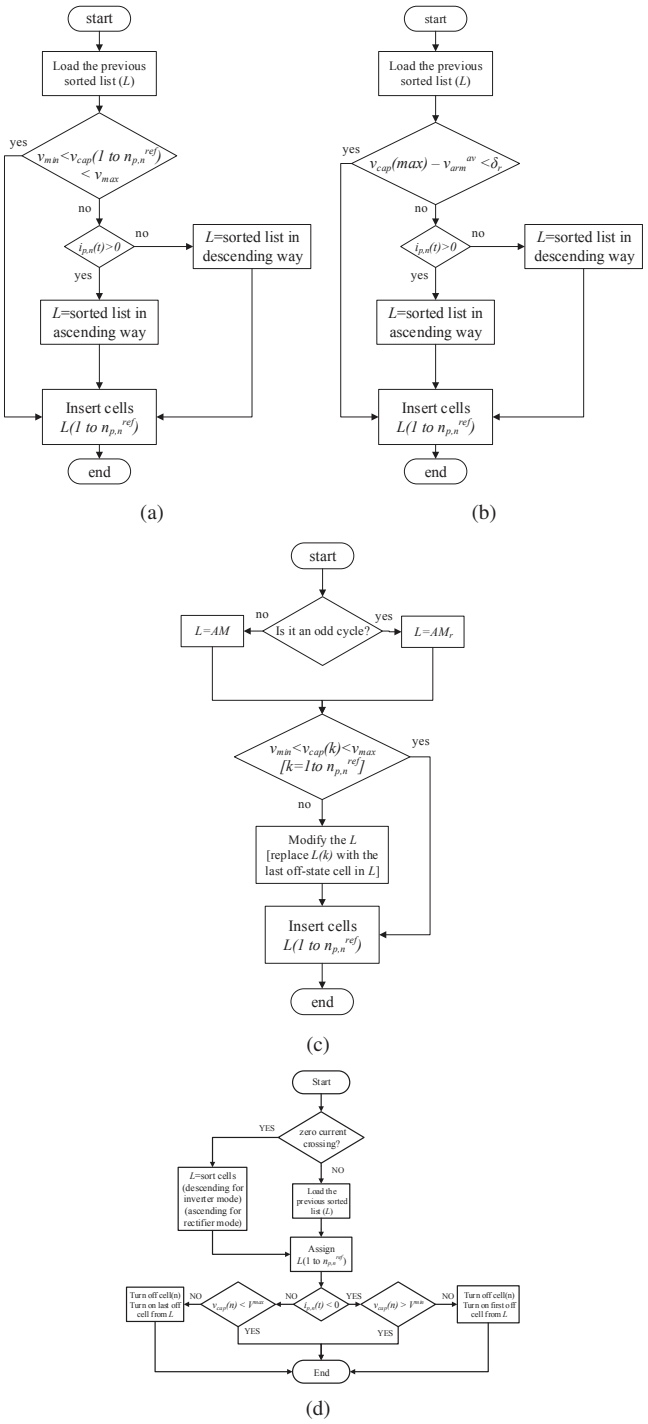

Fig. 3. Tolerance band switching methods (a) Fixed tolerance band and sorting method (*CTBsort*), (b) Tolerance band around the average voltage and sorting method (*ATBsort*), (c) Fixed tolerance band and sequence reversing method (*CTBsequence*), (d) Optimized method of fixed tolerance band and sorting (*CTBoptimised*).

B. Results and Discussion

The introduced equations in Section II-B are implemented in MMC1 converter of the point-to-point benchmark setup, see Fig. 4, to evaluate the semiconductor power losses for

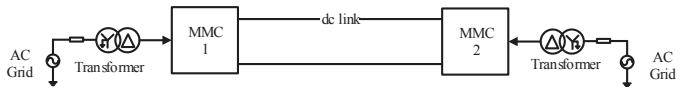

Fig. 4. Point-to-point HVDC link benchmark

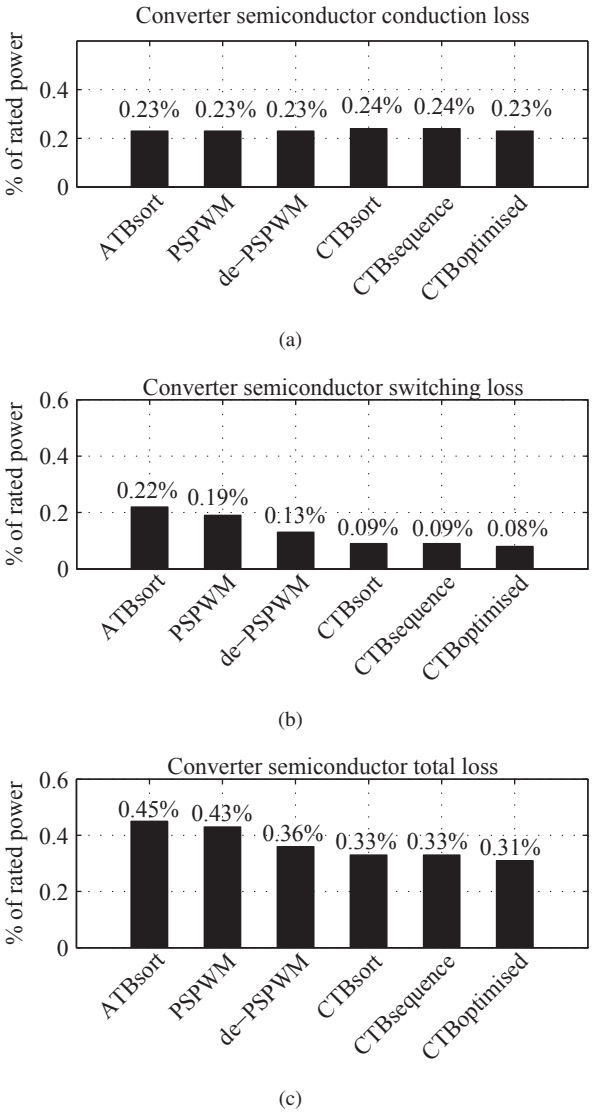

Fig. 5. Converter semiconductor (a) conduction losses, (b) switching losses, (c) total losses

different switching methods. The evaluation conditions are kept similar for all different switching methods. for example, the cell capacitor voltage ripples are maintained to 10% above the nominal cell voltages for all different methods. Moreover, the converter under study transfers the rated power of 1GW at the steady-state condition.

1) Loss performance: Results, Fig. 5, are expressed as a percentage of transferred rated power which is 1GW in this study. However, conduction losses are dominating power losses in all cases. It is observed that most of the switching methods are generating the conduction power loss of 0.23% of

transferred power. On the other hand, semiconductor switching losses vary significantly for various methods. It is observed that considering the average cell voltage as a comparison element for capacitor voltage ripple (*ATBsort*) ends up with the highest switching losses in the converter. Expectedly, the method which consider the current level at switching instant, *CTBoptimised*, lead into the lowest switching loss. Combining both switching and conduction losses indicates that *CTBoptimised* introduces the total semiconductor loss of 0.31% of the transferred power. This is an improvement of 27% in comparison with the conventional phase-shifted PWM method. Note that switching frequencies are varying based on the converter operating point for tolerance band methods which is not the case for carrier-based methods. Consequently, a conclusion can be drawn that tolerance band methods are more efficient in comparison to carrier-based methods.

V. Conclusion

The influence of switching methods on the HVDC semiconductor power loss is studied in this paper. Six different methods are studied in a point-to-point HVDC converter station which is resembling a real HVDC link between France and Spain. According to the loss evaluation, it is shown that utilizing a switching method which considers the current level at switching instants, *CTBoptimised*, can reduce the converter semiconductor power losses by 27% in comparison to the phase-shifted PWM. Considering the switching losses the improvement of 60% is achievable by implementing the *CTBoptimised*. The conduction and switching losses are contributing to the total losses with different contribution weight, depending on the semiconductor characteristics. The semiconductor characteristics can be modified based on the utilized modulation and cell selection methods. The switching loss is much less than the conduction loss for *CTBoptimised*, so a modified semiconductor device can deteriorate the switching loss contribution and have smaller conduction loss instead. In this case the total semiconductor losses can be decreased to a greater extent.

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