

Substation Automation and Protection Division

Line Sectionalizing Using A, PLC And ABB Protective Relays

ABSTRACT: With the advent of utility deregulation, uptime and minimal line restoration times are demanded. With the economics of off-the-shelf equipment usage for substation control and decision making, PLC, and ABB relay use is widely accepted as a restoration solution. This advanced application note explains a method to inexpensively implement advanced Line Sectionalizing techniques using a TPU2000 R, DPU 2000R, PCD 2000, and a programmable logic controller. THE DISCUSSION AND LADDER LOGIC USED HEREIN IS TO BE USED AS A GUIDE TO PLC AND PROTECTIVE RELAY INTEGRATION.

Typical Installation

Figure 1 illustrates a typical installation in which protective relays are installed within a substation providing for restoration schemes. Both the network architecture and sample modified one line is shown for clarity.



Figure 1 -Typical PLC/Protective Relay Report by Exception Application

The scenario illustrated is indicative of a line sectionalizing (load shedding) installation. Using intelligent off the shelf IEDs such as protective relays and PC based HMI interfaces and programmable logic controllers to analyze and perform intelligent switching decisions is more commonplace given the advantages afforded by the economics and increased functionality of such a system. Using an ABB protective relay and a PLC is a logical decision because:

- All items are commercially available Off The Shelf units
- The installations use inexpensive radio modems.
- The software to perform the tasks is programmed in ladder logic, which can be easily written by either a system house or a utility engineer.
- The DPU 2000R, TPU 2000R, or PCD may be field retrofitted by the user, if the Modbus Plus or Modbus protocols are not presently installed in the units.

- No proprietary protocols or equipment is utilized in this installation.
- An inexpensive operation interface allowing for visualization of local and remote status/operation is available.
- Real Time Switching is based on instantaneous decisions made by the microprocessor based IEDs.

As illustrated in Figure 1, the feeder and substation 2 are located a great distance away from the main PLC. Inexpensive radio scatter modems are used to allow communication between the PLC which has the RTU based functionality and logic imbedded within it and the remote IEDs.

Line Sectionalizing Explained

This application note is intended to illustrate the method of obtaining information from the IED's through the Modbus and Modbus Plus interfaces. Each one of the nodes, PLC, IED and HMI operate in concert as follows:

- 1. The PLC reads/writes/calculates information obtained from the TPU 2000R via the Modbus Plus network. Data gathered from the TPU 2000R is:
 - Breaker Status (52a, 52b) is read
 - Cumulative Watts, Vars, 3 Phase Power, Amps, Volts, Watts, Var values are read.
 - Calculation of the combined loading is performed when the Substation Location 1 is feeding the lines at Location 3 (PCD 2000).
- 2. The PLC reads/writes information between itself and the DPU 2000R. Data gathered by the PLC is:
 - Breaker Status (52a, 52b) is read.
 - Cumulative Watts (per phase and 3 phase), Vars (per phase and 3 phase), Amps, Volts, frequency values are read.
 - Calculation of the combined loading is performed when the Substation Location 2 is feeding the lines at Location 3 (PCD 2000).
 - Control Operation capabilities such as breaker trip and breaker close can be completed automatically (via logical decisions made by the PLC) or manually (via an operator at the HMI station).
- 3. The PLC reads/ writes information between itself and the PCD 2000. Data gathered by the PLC is:
 - Breaker Status (52 a, 52 b) is read.
 - Cumulative Watts (per phase and 3 phase), Vars (per phase and 3 phase), Amps, Volts, frequency values are read.
 - Control Operation capabilities such as breaker trip and breaker close can be completed automatically (via logical decisions made by the PLC) or manually (via an operator at the HMI station).
- 4. The MAGELIS HMI displays the data values held in the PLC. In this installation, the PLC acts as a data concentrator and arbitrator for the logic operations. The MAGELIS HMI can disable the automatic restoration functions preprogrammed in the PLC. With the PLC placed in manual control mode, the operator viewing the data on the MAGELIS screen can perform manual restoration since visualization of each breaker and all feeder metering values are displayed on the screen.

There are two modes of operation, MANUAL and AUTOMATIC restoration. With the system in AUTOMATIC mode, line restoration is performed by the PLC without any operator intervention. AUTOMATIC MODE operation occurs as such:

- 1. The breakers at Substation Location 1 and Feeder Location 3 are closed. The breaker at Substation Location 2 is open. In this example, the feed from the TPU 2000R is providing supply to the feeder at location 3. The PLC is constantly reading metering values and calculating the average load required by Feeder Location 3.
- 2. On the event of a fault, the TPU 2000R trips the breaker. The PLC recognizes the trip immediately (under 10 mS in this case) and immediately determines if sufficient reserve is available at Substation Location 2 to supply Feeder Location 3.
- 3. The PLC immediately opens the breaker at Feeder Location 3. The PLC verifies that reading the status of the breaker opens the breaker. The MAGELIS system immediately displays the metering values and breaker status on its screen and may also generate alarms to alert the operator or attached SCADA system.
- 4. If Substation Location 2 has sufficient reserve to supply the feeder at location 3, the PLC wait 3 seconds to ensure that the TPU at Substation Location 1's breaker is open, AND that the Breaker at Substation Location is also open.
- 5. The PLC shall Close the breaker at Substation Location 2 and read the metering values and breaker status reported by the DPU 2000R.
- 6. The PLC still calculates the load on the line and determines if there is still sufficient reserve to add additional feeder lines, the PLC shall wait another 1 second and send a close command to the breaker controlled by the PCD 2000.
- 7. The PLC shall read the metering values and breaker statuses at each of the 3 IED locations and report them to the MAGELIS system via the internal network at the substation.
- 8. At each of the above steps, a message is generated as to the step being performed by the PLC. The status of each step (along with any error) messages is displayed and archived by MAGELIS operator interface. The PLC will place the restoration scheme in MANUAL mode, so that an operator may place the system in the same state that it was in prior to the TPU 2000R trip.

IF any one of the steps fails to execute, the MAGELIS HMI will display an error message as to the cause of failure in the restoration process.

MANUAL MODE disables the PLC's capability to trip/close the breaker. The PLC still computes the loading values and alerts the operator as to alarms. The PLC also communicates with MAGELIS MMI and displays messages/ breaker status information/metering data informing the operator if adequate load is available to supply the feeder. This gives the operator additional information if a manual restoration is to be performed via the operator interface. Additionally, the operator commands may be sent directly to the PLC to perform manual trips and close commands.

Method Of Implementation

Two Ladder Logic instructions within the Modicon PLC allows line sectionalizing to occur:

- MSTR obtains the data from the TPU relay. Once the data is obtained, the PLC determines the field conditions and decides upon the control to be performed.
- XMIT instructions when executed by the PLC, initializes the COM port resident on the unit. The PLC can then act as an Remote Terminal Unit (RTU). The PLC then interrogates the DPU 2000R and PCD 2000R to determine if the units are available to be switched.

The remainder of this application note explains the programming process and ladder logic required to implement the application pictured in Figure 1.

Obtaining Relay Information Via MODBUS Plus And MODBUS

The PLC is programmed using four ladder logic segments. The logic within each segment is as follows (for this example).

SEGMENT 1: READ TPU 2000R VALUES VIA MODBUS PLUS. PROVIDE MANUAL TPU CONTROL OPERATIONS VIA MODBUS PLUS.

SEGMENT 2: READ DPU 2000R AND PCD 2000R VALUES VIA THE RADIO MODEMS USING MDOBUS PROTOCOL. PROVIDE MANUAL AND AUTOMATED CONTROL OPERATIONS VIA MODBUS.

SEGMENT 3: LOGIC REQUIRED FOR EACH STEP IN THE RESTORATION SEQUENCE FOR CALCULATION AND CONTROL. HMI LOGIC FOR TRIGGERNG MESSAGES AND ALARMS IN THE MAGELIS SYSTEM.

SEGMENT 4: ANCILLARY SUBROUTINES providing 32 bit number conversion since the Compact 984 does not easily allow for mathematics on a double register number or single register number containing a value of 9999 or greater. The ABB products allow numbers to be reported in a single register interpreted as 0 to 65535 (Unipolar) or -32767 to 32768 (Bipolar). If a number is a 32 bit representation, PLC logic must be added to the specific vendor's PLC allow computations to occur.



Figure 2 - Modbus Plus Ladder Logic Implementation Strategy.

The Ladder Logic is Segment 1 is very straight forward. Figure 3 illustrates the method of obtaining the data from the TPU 2000R via Modbus Plus.

The data requested includes logical element status which includes breaker trip information for phases A,B, and C. The phase information is latched, and its status must be reset by the operator to annunciate the alarm which is decoded by the PLC.



Figure 3 - Data Map Request from the Compact PLC and TPU 2000R via MODBUS Plus

The MSTR block logic follows.

Utility	Elements Edit	Ga/Srch	Network	Befs	Tools	Quit
CDENO_S	F3 F4	-75	16	-F7-Lev B	-F8-0F7	-19
Seg. 1 #1 1	Reset MSTR on FIFU	upon entry				
	()-					
00112 0010	2 09198					
- C						
L_CHD_GOEDE_EI	PTY All commands in	the QUEUE :	SENT.			
	Re	ference Da	ta ——			
Parmet Dec	0001	Bantra	1.14			
	ULTING OF LING	anding o	-			

Figure 4 - Network 1 Ladder Logic (MSTR Modbus Plus Logic)

NETWORK 1 – FIGURE 4:

The logic is written with cyclic polling occurring to gather the data and place it in a 4X memory space as illustrated in Figure 3. If a command is to be initiated via the ladder logic program (AUTOMATIC RESTORATION) or via the operator interface (MAGELIS), a specific request pointer is placed into a FIFO buffer for immediate execution once the present command is executed by the MSTR block.

Network 1 senses that a pending command is to be executed in the FIFO block and the current command is terminated in the cyclic polling sequence for the MSTR block.

Jtility	Elements Edit	Go/Srch	Network B	efs 1	001s	Quit
Seg. 1 82 ; 2 1 09112	00105 #0006 40164	00133 00131	-10	7-Lev 6-1	0- <u>UM</u>	a
01660 66109	00131	[0005 0013	3		- 120
00109	40164 #00990 SUB 40239		10164 SUB 10239	40164 #0001 SUB 40165-	10165 10996 MUL 40166	00134
L, CHO "ÖNENE" EHB.	TY All commands in t Ref	he QUELIE : exence Da	sent. ta	153472340		
Remote the day	-) 04614					

Figure 5 – Network 2 Segment 1 – Cyclic Poll Logic Block

NETWORK 2 – FIGURE 5:

There are 6 cyclic poll read instructions (illustrated by FIGURE 3 ABOVE). This network actuates the time to send each of the six instructions to the MSTR block to read the information from the TPU. If an instruction must be executed (such as a TPU TRIP, RESET TARGET LED Instruction) which is not part of the cyclic instruction sequence, this drum sequence is halted until all the commands in the buffer are executed by the MSTR instruction. When the FIFO is emptied, then cyclic polling resumes and this logic construct is energized.

NETWORK 3 – FIGURE 6:

As illustrated in figure 3, all instruction parameterization registers for the MSTR instruction is stored in the compact 6X memory registers. This network instruction (upon a change of the CTR instruction's cyclic poll) reads the block in 6X memory and places it in 4X memory. The contents are then moved into the MSTR block. Register 40100 = a 2 (read instruction) or a 1 (write instruction) based upon the data being read or written to the TPU. Registers 40102 through 40107 contain the MSTR parameters for the routing address (in this case the TPU is Address 1 Path 1) and such information as the number of registers to be transferred/read and the address in the TPU (to be read or written).

001111tg Sey. 1 13 1 1 00134	Elements Ed 13 PA WRITE 6X POINT 40167 40229 40230 40120	lit Go/Srcl P5 TER DATA TO REA	h Network PD AD	Refs 17 Lev (Tools Tools	Quit.
-	[BL39] {X980 #0001 #0001	40170 19100 BLim #9661	40171 10102 88.84 8005			
estri_cycle_	cont	— Reference 1	Data ——			
Format :Decir	ial OFFII	ne Range	s : 1			

Figure 6 - Network 3 Figure 6 –6x Pointer Data

NETWORK 4 – FIGURE 7:

This is the MSTR send instruction which is parameterized for read and write commands. The upcounter in the logic counts the number of good network transactions (00104 energizes on a GOOD communication and 00103 energizes on a bad communication, 00102 is the instruction active indication). It should be noted that although 125 registers may be read/written at any one time, the program has been limited to Modbus Plus data accesses of 30 registers (to conserve PLC memory). The data is stored in 4X memory 40110 through 40149.

Utility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
1 00000 Sey. 1 #4 1 00000 00100	00113 00107 40100 001 00107 40100 001 0 40110 001 #8510 001 801)	-0	-F7-Lev	8-19-011-	
Format :Dec	001 B	of exence De Bange	ita			

Figure 7 - Segment 1 Network 4 – Master Polling Block

NETWORK 5 – FIGURE 8:

The UCTR in this network counts the BAD Modbus Plus network transfers (an excellent indicator for network troubleshooting and program troubleshooting). This network also determines when an network access has finished executing. The TMR in this network construct places a dwell time of 200 mS between each Modbus Plus network transaction.

Utility	Elements	Edit	Go/Srch	Network	Refs	Tools	Quit
Sey. 1 #5 5 Sey. 1 #5 5 Seites Seites 99116 01099	P3 Cyclic Time (#0100 001 UCTR 40169	F1 Schedules)— 16	rs	-16	-17-Lov (3-76-0 77 -	-19
00112	000 00100	05 00103	00104 40140 T.01 40111	01000		() 60197	_
Ľ		11-2	De De				
- Format : Ber in	43 Of	lline	Bance	. 1			

Figure 8 - Ladder Logic Dwell Timer and Bad Transaction Network

NETWORK 6 – FIGURE 9:

This network determines if the FIFO has an entry. If the FIFO is empty Coil 00112 is energized. If the

FIFO is full Coil 00111 is energized. The FIFO can contain 19 pending commands for execution in the TPU. As illustrated in Figure 3, the commands are numbered 1 through 10. 40142 and 40143 respectively are the data pointed to in the queue and the FIFO queue pointer.

Coil 00109 is the indicator for the program that the FIFO has an entry and the master should be halted.

Utility	Elements Edit	Go/Srch	fictuork	Refs	Tools	Quit
1 00210 5 Sey. 1 86 1 6 10143	- <u>P3</u> -P4- is Write Cmd or Cy 	r5 cle Read	-16	-17-Lev	8-10-011-	-19
40142 FOUT #8019	00111 00112 00112 00112					
00100 00103	00112 00102 001	05 00109				
		eference Da	ta —			
	7.50 					
 Format (Decimation) 	u urrine	Nange	1			

Figure 9 – FIFO MSTR Halt Logic

NETWORK 7- FIGURE 10:

This network delays the initiation of the MSTR block send instructions when a FIFO command has been sensed in the buffer. The pointer to this command is in the 40163 pointer register. The delay is 100 mS. As can be seen in the ladder logic, the FOUT (FIFO out stack) is popped and the parameters corresponding to the FIFO pointer are transferred to the logic to transfer the 6X MSTR pointers from the 6X registers pointed (in FILE 1 6X memory) to the MSTR 40100 through 40109 register block.

Utility	Elenents Edit	t Go/Srch	hetwork	Refs	Tools	Quit
F1 EDEND_5 [Sear. 1 07 1 7	F3 F4 Tincout-expired	Load MSTR	-16	-17-Lev	8-re-orr-	-19
「「「「「」」」	Internal Contract	00111				
00100 00112	47.01	00114				
	465491	121			-	
		00114	40143 40	142 001	15	
			10142 10	163		
			FOUT - B	Lin		
			40015- 80	001-		
1						
	and a Berry and					
<pre>* mstr1_cycle_)</pre>	alteauriru has o	- Reference D	ata —	TFU		
Format :Beci	al Offlin	e Range	: 1			

Figure 10 – Network 7 Segment 1 – FIFO Scheduling Halt Logic

NETWORK 8 – FIGURE 11:

This is the 6X transfer instructions as illustrated in FIGURE 11

Lility CDEMO_5	Elenests Edit	Go/Srch	Network P6	Refs 17 Lov	Tools <mark>6 78 011</mark> -	Quit
00115	10153 1022 10153 1022 10001 1000 1012 10225 1022	5 40227 6 40239 8 80001	10228 40170 XMRD #0001	901 901 901 [III 100	70 90171 60 40162 399 18139 01 80006	
	He Re	ference Da	ita			

Figure 11 – Ladder Logic 6x Transfer Instructions.

The method to transfer the logic and the file layout in 6X memory is as such:

File 1 – Registers 60000 to 604999 contain the MSTR 1 instruction command parameterization. The commands are in a block of 6 register formats.

60XXXX+0 = MSTR Command 1 = read 2 = write 60XXXX+1 = Number of registers read/written 60XXXX+2 = Address in TPU to be read/written 60XXXX+3 = Node Route 1 Address 60XXXX+4 = Node Route 2 Address 60XXXX+5 = Node Route 3 Address

Routing address Paths 5 and 4 are a value of 0.

FILE 2 6X registers are the data written to the TPU. Each command is in a block of 10. If the command in the corresponding block is 1 (read) then the file 2 block of registers is a don't care. If the command in the corresponding block is 2, then the data in FILE 2 with the corresponding configuration data in FILE 1 is sent to the MSTR configuration registers. FILE 2 data is transferred to 40110 (MSTR data field). The grouping of the data in file 2 is always:

61XXXX + 0 to 61XXX + 9 = Block data.

Utility	Elements Edit	6a/Srch	Network	Refs	Tools	Quit
2 - 40130 - 9 I 9 5 cg. 1 + 9 I 9 I 9 00115 - 40100 - 1500 - 90239	40163 4024 40163 4024 10001 10001 10001 10001 1000 4024	9 90292 9 90292 9 90295 1 80001	90243 90110 10001	-f7-Lev F	PB-OFF-	-13
	Be	ference Da	ta —			
Format (Decimal	i Off Line	Bange	; 1			

Figure 12 – Transfer Logic For Control Instruction Parameterization

NETWORK 9- FIGURE 12:

As explained above, if the pointer in the FIFO vectors to a control instruction, then the FILE 2 data corresponding to that pointer must be transferred to 40110 in the MSTR instruction. This network does just that. The 6X address is calculated by the MULT instruction and then passed as an argument to the XMRD instruction. Upon execution of the XMRD instruction, the data is transferred into the MSTR block. If the FIFO instruction in the buffer is a WRITE instruction, then the pointer placed in the buffer is multiplied by 10 to get the block of data to transfer to the MSTR data register buffer 40110. The multiplier for instructions are:

PTR = 1 Block 0 Add 0 to pointer for FILE 2 60000 PTR = 2 Block 1 Add 10 o pointer for FILE 2 60010 PTR = 3 Block 2 Add 20 pointer for FILE 2 60020 PTR = 4 Block 3 Add 30 to pointer for FILE 2 60030 PTR = 5 Block 4 Add 40 to pointer for FILE 2 60040 PTR = 6 Block 5 Add 50 to pointer for FILE 2 60050 PTR = 7 Block 6 Add 60 to pointer for FILE 2 60060 PTR = 8 Block 7 Add 70 to pointer for FILE 2 60070

... and so on, and so on

NOTE – The data is transferred if the function code in 40100 = 2 (write), else the data is meaningless.

NETWORK 10 – FIGURE 13:

This network is only a latch in which once the buffer FIFO contains an entry.



Figure 13 – Segment 1 Network 10 – Start Polling Sequence

NETWORK 11 to 19 - FIGURES 14 to 22:

The commands 1 through 5 are the cyclic ladder logic commands which read

- REG 40129 TPU STATUS
- REG 40385 40401 CURRENT ANGLE DATA
- REG 40513 40518 VOLTAGE ANGLE DATA
- REG 40528 40533 POWER VALUES

• REG 41153 –41156 ALARM STATUS VALUES

The Command 6 is the trigger command for all the WRITE commands which include

- TRIP COMMAND Write 41411 41415 and WRITE 41410
- RESET TARGETS Write 41411 41415 and WRITE 41410
- RESET ALARMS Write 41411 41415 and WRITE 41410
- RESET LATCHED DATA Write 41411 41415 and WRITE 41410

The commands as illustrated in FIGURE 3 of this document.

Otility	Elenents I	Ait	Go/Srch	Network	Refs	Tools	Quit
Sey. 1 11 1 99140 16091 10099 SUB 40224	49224 49143 1710 READ ST 49224 49143 1914 1914 1919	TATUS DA	TO Th	10	- <i>er</i> -Lev c	10-011	-12
Forest :Decir	ns	Ref	erence Da	ta			

Figure 14 – TPU Read Status FIFO Pointer Load Logic



Figure 15 – TPU Read Currents FIFO Pointer Load Logic

Utility	Elenents	Edit	Ga/Srch	Network	licfs	Tools	Quit
Seg. 1 013 1	13 VOLTAGES	TPU 20008	10	-10-	-17-Lev 0	-re-um	-12
	Illing						
00142 1000	3 90224						
1000	9 49143						
SUB 40722							
104LL							
ll.							
100000000000000000000000000000000000000	1000						
C TPU_READ_U0	LTAGE	- Bef	erence Da	ta —			
Format (Boo)	usa ne	filine :	Bancos	- 1			
Furnets ales	1601 08	11100	nalage				

Figure 16 – TPU Read Voltage FIFO Pointer Load Logic



Figure 17 – TPU Read Wattage FIFO Pointer Load Logic



Figure 18 – TPU Read Alarm Status FIFO Pointer Load Logic

Utility	Elenents	Edit	Ga/Srch	Network	Refs	Tools	Quit
2 20270.5 Sey 1016 10 00145 40007 0009 SUB 465224	73 7PU 20968 40224 40143 FTN FTN 0019	P4 Belay Tr #0006 #00006 SUB 40224	FS ip Instr. 40224 40143 FIN 80019	F6	-17-Lev 8	-F8-011	
· IPU_TRIP_BREAD	ски	Bef	erence Ba	ta			
- Format :Decima	61 OF1	line	Bange	: 1			

Figure 19 – TPU Trip Breaker FIFO Pointers Load Logic

Utility	Elements I	Mit	Ga/Srch	Network	Refs	Tools	Quit
1 00280 5 Sey. 1 017 1 17 30146 #0008	Elements I -P3	4 16587 Tel 10996 10996 10996 SUB	49224 49143	network 26	Not's		Quit 19
402243 1	00194	40.224-	680154				
TPU_RESET_TABGE	ETS		2012/02/201	24			
		- Here	seence Ba	ta —			
Proved Provide							

Figure 20 – Reset Targets FIFO Pointers Load Logic

Utility	Elements E	lit Go/Src	h Network	Ref s	Tools	Quit
Seg. 1 018 1	18 RESET TPU200	OR ALARMS DAT	10			
00147 10009	40224	#0006 90224				
#0000 ISUB	40143	40143 ISUB 1218				
10224	#9919	40224 #0019	μ			
	1000					
<pre> TPU_RESET_AL </pre>	aans	- Reference	Data —			
L Format :Deci	nal Offici	ine Rang	e : 1			

Figure 21 – Reset Alarms FIFO Pointers Load Logic

Utility	Elements E	lit G	ia/Srch	Network	Refs	Tools	Quit
Sey. 1 #19 19 00148 #8019	10221	10006	49224 49143		-27-689 0	-ro- <u>urr</u>	
3UB 40224	FIN #9915	SUB 40224-	FIN				
-							
TPU_RESET_SYS_	STAT	Befer	ence Dat	ta			
Fornat (Decina	1 02£1	ine	Bange	1			

Figure 22 – Reset Latched Points FIFO Pointers Load Logic

NETWORKS 20 to 24 – FIGURES 23 to 27

Once the data is read from the relay using the cyclic reads (pointers 1 through 5) or via the FIFO commands, the data read must be transferred from the MSTR read buffer to a general buffer for retrieval from the PLC. The PLC then serves as a data concentrator. The TPU data registers are contained in 41700 through 41726. The ladder logic networks in this construct are triggered when the MSTR instruction has obtained the information from the relay. The instruction then transfers the appropriate quantity to the appropriate registers (as illustrated by FIGURE 3 above).

The SUB instruction determines the MSTR command executed and the BLKM command instruction block moves the information from the MSTR data buffer (40110) to the appropriate register location from 41700 through 41726 resident in the PLC.

Utility	Elements	Edit	Ga/Srch	Network	Refs	Tools	Quit
1 80370 5 Seg. 1 820 1 2	F3 0 Read In Cy	r4 clic Pol	-P5 I Data	-16	-17-Lov	8-re-orr-	-19
00104	49164 89901 SU8 40239	40110 41790 BLKM 10001					
01000 N 00104 40163		40110	40163				
#0001 SLB 16239-		41700 BLKM #0006	40163 X08 #8661				
are a possible		- Bef	erence Da	ita —			
Format Therin	-1 DEF	11.00	Benro	- 1			

Figure 23 – Read In Reply To Status Data Request And Store In PLC Registers

Itility	Elenents	Edit	Go/Srch	Network	Refs	Tools	Quit
Seg. 1 #21 1 2	I Read in T	PU ZOOBR I	Winding C	lurret	TI-DOV	0-ro-0rr-	
00104	49164	40110					
	#0002	41701					
	40239	BLRH #0016-					
91660			i l				
00104 40153		40110	49163	-()- 60161			
			Lanco L				
SUB		BLKM	X08				
402394 mstr1_DOME		#0006-	, #00011				
		- Ref	erence De	ita —			
Format :Decim	al 06	fline	Range	: 1			

Figure 24 – Read In Reply To Phase Current Data Request And Store In PLC Registers

Utility	210_5	Elenents	Edit F4	Go/Srch	Network	Refs	Tools	Quit
Sey 1 17 99104 01900 09104 4	2 1 22 0163 0003 508 0239	TPU 20008 90164 90003 SUB 90239	4011age 40110 41717 BLRH 40006 40110 41717 BLRH 80006	49163 49163 49163 80001	—()— 60152			
Format :	Decina	1 064	line	erence De Range	ita			

Figure 25 – Read In Reply To Phase Voltage Data Request And Store In PLC Registers



Figure 26 – Read In Reply To Wattage Data Request And Store In PLC Registers

Utility	Elements	Edit	Go/Srch	Network	Refs	Tools	Quit
Sey 1 22 2 09104 09104 09104 001000 00104 00105 00005 00005 00005 00005 00005 00005 00005 00005 00005 00104 001000 00104 001000 00104 001000 00104 001000 00104 001000 00104 00005 00104 00005 00104 0005	40164 10005 40239	40110 40110 41723 81.84 4004 40110 41723 81.84 80006	Eatee Eatee Eatee Eatee Eatee Eatee				
Format :Decim	al Off	Refe	Range	ita			

Figure 27 – Read In Reply To Alarm Data Request And Store In PLC Registers

Segment 2 – Data Gathering From The PCD 2000 And DPU 2000R.

The DPU 2000R and the PCD 2000 are both located some distance from the PLC. Attachment to these relays is accomplished using simple SCATTER RADIO MODEMS. The radio modems are able to communicate over a distance of 15 miles and retrieve information from them via a 10 bit protocol. The SCATTER RADIO MODEMS have the advantage that no special licensing is required for connection to the devices.

The ladder logic required for data retrieval is located in the ladder logic segment 2 and is based upon the XMIT instruction which turns the PLC's RS 232 port into a MODBUS master. This enables the PLC to query attached devices and poll for data. In this way the PLC is able to determine the loading of the remote feeder and breaker status of the feeders being monitored and protected by the DPU 2000R and the PCD 2000.

The PLC queries both the PCD and DPU via the command parameterization of the XMIT instruction. The topology of the installation is illustrated in FIGURE 28 as follows in this discussion.



Figure 28 – Network Topology For Nodes Remote To The PLC And Polled Via MODBUS Command Responses

The ladder logic shall be reviewed for the method to complete the data exchange between the PLC and the IED's

SEGMENT 3 NETWORK 1:

The FIFO used to gather the information from the IED's is reset whenever data is transferred into the FIFO for polled queue. This is a standard instruction construct which is similar to that used for the MSTR instruction.

Utility	Elements Edit	Go/Srch Metwo	rk Refs	Tools	Quit
1 30370_5 Sey, 3 #1 1 26 30312 90392		F5 F6 F- Reset Unit	I7-Lev	8-re-orr-	-19
Ho Symbol/Desc	riptor available	ference Data —			
- Format (Decim	al Offline)	Range : 1 —			

Figure 29 – Segment 3 Network 1 – FIFO Entry For XMIT Instruction Notification

SEGMENT 3 NETWORK 2:

The network is a cyclical poll which pages the 10 instructions to the XMIT to gather data from the two IED's (PCD 2000 and the DPU 2000R). The UCTR instruction increments between 1 and 10. The Pointer is then multiplied by 10 (stored in 40333) which serves as the pointer to the 6X command buffer which parameterizes the XMIT instruction to retrieve the IED's data.

Utility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
1	7 XHIT Cyclical Poll 00306 #001 4033	-15 	- ro - : - :	-17-Lev 8	-re- <u>orr</u> -	0
01000 00309	00331 1033 1000 1000 1000 1000 1000 100	0 0 9	10011 000 10330 SUB 10239	P - 333 4633 	10331 10010 11 10010 11 100332	00334
"No Synbol/Desc Format :Decir	riptor available Re	ference De	: 1			

Figure 30 – Segment 3 Network 2 – Cyclic Poll Pointer Setup Logic

SEGMENT 3 NETWORK 3:

This network seems to be rather complex, but it really is not. The XMIT block needs two types of parameterization 1). parameterization of the block for delay parameters, timeout parameters and definition of pointers for the MODBUS data gathering which is in registers 40308 through 40315. 2). the parameterization of the Modbus commands which are pointed to by registers 40309 and 40310 (which is the address of the 5 registers for command parameterizations) and the length of the parameter block (which is 5 and its structure depends upon the instruction, please reference the MODICON XMIT BLOCK documentation for a more complete discussion of the data).

The XMIT instructions are stored in FILE 2 and FILE 1 of 6X memory beginning at addresses 600500 and 610500 respectively. File 1 parameterizes the XMIT block parameters and FILE 2 parameterizes the particular MODBUS request. The mathematics of this block calculates the data in the following way:

FILE 1 POINTER (Reg 40334) = Pointer (Reg 40331 * 10) + 500 offset. FILE 2 POINTER (REG 30337) = Pointer (Reg 40331 * 30) + 500 offset.

The File 1 pointer is passed to the XMRD block which transfers 7 registers to the XMIT parameterization space 40308 to 40315. The File 2 Pointer is passed to the XMRD block which sends 30 registers from 6X memory to 40355 to 40384. FIGURE XX illustrates the parameterization which must occur in order to allow the XMIT block to gather the data successfully. As is illustrated in FIGURE 31 the PLC stores the data in PLC register 41700 through 41849. The PLC program has been optimized for data storage and grouped register usage. This program may be expanded to perform other functions.



Figure 31 – XMIT Parameterization Philosophy For Data Control.

Utility 1 CDENO Sey. 3 #3 1	Elements 5 13 28 XHIT Cyclic	Edit F4 al Poll	Go/Srch	Network 10	ilefs 17-Lev	Teols 8-re- <mark>0rr</mark> -	Quit 19
00334 4033 #054 AD 4033	33 40331 403 99 #9936 #850 9 MUL AM 34 40335 4833	16 40334 10358 10358 18LKM 17 #0991	40348 40338 (XH8D #9661	- 40338 40 40308 40 101,00 40	1337 463 1367 403 11.811 121	85 55 80	_
Format :Des	cina] Off	Refe	arence De Range	1ta			

Figure 32 – Segment 3 Network 3 – 6x Pointer Computation Logic For Loading XMIT Instruction

SEGMENT 3 NETWORK 4:

Network 4 is the base XMIT instruction. As illustrated above, the data table is filled when the drum timer of Segment 3 network 2 counts between 1 and 10 (which are the cyclic read instructions. An optional UPCTR counts the good transmissions (which is good for keeping track of communication percentage failures) over the radio network. This is used with the next nework in the segment to keep track of the type of failures occurring during troubleshooting of the program. The Ladder Logic follows and is illustrated in FIGURE 33.

Utility	Elements Edit	60/Srch	Network	Refs	Tools	Quit
Seg. 3 #4 i 29	Send Corenants to De 00313 00307 #0001 0030 40300 0030 2011 0030 0030 0031)	_() 00310			
-	Bel	erence Da	ta —			

Figure 33 – Segment 3 Network 4– XMIT Instruction And Good Transaction Count

SEGMENT 3 NETWORK 5:

This network latches the last XMIT error in register 40300. It is reset by pulsing coil 00888. This is additional logic added for the ease of troubleshooting the program. The logic is illustrated in FIGURE 34.

Utility	Elenents Edit	Go/Srch	Network	Refs	Tools	Quit
1	BROR LATCH	00669	40301	-17-Lev	6-ro-urr-	
66839 P ee838 P e1099	40838 40838 XUR #0001		[BLRH] #6091			
ⁱ Åa Synbol∕Descri	ptor available Bof	erence D	ata			
Format :Decimal	Offline	Range	: 1			

Figure 34 – Segment 3 Network 5 – XMIT Error Bad Transaction Counter And XMIT Error Latch Clear Logic

SEGMENT 3 NETWORK 6:

The output of the XMIT block signals when an error occurs on a transmission. The UCTR instruction in this logic construct counts the number of transmission errors experienced by the XMIT BLOCK. This is instructional in determining the amount of errors occurring on the network.

The second logic construct (with the TMR) places a dwell time of 100 mS between MODBUS transmissions. The coil 00307 pulses the XMIT instruction when the FIFO buffer is empty and the XMIT instruction is able to transmit and instruction as part of its cyclical poll structure. The ladder logic is illustrated in FIGURE 35.

Itility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
Seg. 3 16 31	Check QUEUE #9999 00316 40393	-	10		0-ro-urr	-9
00312	00309 00306 00303 00307 01809 00392	99394 49394 T.01 49395	01000 00		() 60307	-
	- Ref	erence De	ita —			
- Format :Decim	al Offline	Range	: 1			

Figure 35 – Segment 3 Network 6- XMIT Dwell Timer And Bad Transmission Counter Logic.

SEGMENT 3 NETWORK 7:

As with the Modbus Plus MSTR Logic, another FIFO has been constructed in which a manual control (or automated control instruction initiated by the ladder logic may be performed). Note the FIFO may contain up to 19 control instructions which may be queue'd for processing. Additionally, note the trigger construct for pending FIFO commands to be sent to the XMIT block (coil 00309) interrupting the cyclical poll. Using

this philosophy ensures that control commands and operator initiated commands are immediately scheduled for operation by the XMIT block.

Utility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
1 20270 Sey. 3 7 7 40397 40397 10019 10019 00308 00308 00309	2 0911 FIFD Check 5 09111 0 03112 00312 00312 00312 00312 00312 00312 00312 00312 00312 00312 00312 00315 005 005 005 005 005 005 005 0	() ; 00309	- PD	-77-1499	8-76-077-	-13
		erence Da	ta —			
Format :Deci	ima] Offline	Bance	: 1			

Figure 36 – Segment 3 Network 7 – FIFO Empty/Full Notification Logic

SEGMENT 3 NETWORK 8:

If the FIFO has data, this logic construct interrupts the polling of the XMIT instructions and immediately parameterizes the block with the parameters pointed to within the FIFO queue. A dwell time of 100 mS creates a pause for the XMIT instruction to terminate. The logic in SEGMENT 3 NETWORK 9 creates the pointers for obtaining the 6X register data for passing to the appropriate 4X XMIT parameterization registers. FIGURE 37 illustrates the logic to accomplish this task.

Utility	Elenents	Edit	Go/Srch	Network	Refs	Tools	Quit
Sey. 3 #8 3 00309 00312	3 XHIT FIFD 09313 #99 17. 404	10 10 11 17	- Stop B1 () 00314	ocik	-17-1494	<u>6-re-urr</u> -	- 1 2
			00314	40397 40 10395 40 FOUT - 8 #6019 #9	396 003 418 Lkm 901)— 115	
Ha Synhal∕Des	criptor avai	lable Ref	erence Da	ta			_
Format :Deci	nal Of	flime	Range	: 1			

Figure 37 – Segment 3 Network 8 – Cyclic Poll Cessation Logic

SEGMENT 3 NETWORK 9:

As illustrated, this is essentially a copy of Segment 3 Network 3 logic. It is copied here in order to keep the same philosophy for instruction parameter loading whether it is from a cyclic poll request or a FIFO task interruption. The logic is shown in FIGURE 38.

0tility 7100840_5 [Seg. 3 #9 1 34	Elenents Ed 13 P4 transfer FIFO	It Go PTH data	/Srch to uni	Nctwork R 16 t	cfs <mark>-Lev 8</mark> -	Tools FB- <mark>DFF</mark>	Quit -P9
90315 0418 #0010 MIL 40332	40333 40418 10500 10030 100 1401 40334 40335	40336 4 #0500 4 ADD 1 40337 #	0334 4 0421 4 BLRM 1 9661 8	0419 0330 KMRD 40330 140330 10000 10000 10000	8 103377 8 10128 9 10128 9 18.301 7 #0001	10126 10355 XMR0 10991	- -
No Symbol/Descr	iptor availab	le Befere	nce Dat	1			

Figure 38 – Segment 3 Network 9 – XMIT Pointer Computation Logic

SEGMENT 3 NETWORK10:

This network determines that the FIFO is empty and cyclic polling using the logic in Segment 3 Network 2 resumes. The Logic is illustrated in FIGURE 39.

tility	Elements Ed	lit Go/Srch	Network	Refs	Tools	Quit
eg. 3 #10 1 3	S FIFU DATA AL	I Cleared.	-10	-rr-Lev	8-n-urr-	-0
99340 30393	09304 91609	80313				
00313						
		00313 00312		()-		
		00010 00010		090		
o Symbol/Desc	riptor availab	le				
		- Reference D	ata ——			
Format :Decim	al 0001i	ne Range	: 1			

Figure 39 – Segment 3 Network 10 – Resume Cyclic XMIT Poll Logic

SEGMENT 3 NETWORKS 11 THROUGH 20.

As illustrated in FIGURE 31 – The first 10 instructions in the buffer are to read data from the Modbus registers in the DPU or PCD and stack them in the PLC for later data processing to perform the load shedding/load restoration (line sectionalizing). Figure 31 illustrates in the FILE 2 explanation, that whenever the POINTER from number 1 to 10 is placed in the FIFO (if an interrupt command is required) or if the UCTR instruction in Segment 3 Network2 changed within it's sequence, the data is transferred as illustrated. Networks 11 through 20 perform the following:

- If the SUB and FIN combination logic construct is energized by the preceding contact, the FIFO is filled with the queue'd command for processing by the XMIT block. This stops the cyclic polling (if occurring) and schedules the command for execution in the next 100 mS/
- When the XMIT block executes and receives the successful transmission, the data received is transferred from the XMIT block buffer and transmitted to the PLC data storage buffer

41750 through 41850. The data may be viewed by an operator interface such as MAGELIS, stored for further processing (decisions on whether to perform the line sectionalizing), or stored in other memory areas for data buffering/concentration for transfer to a host device at a later date.

The contact to the left of the rail (1st logic construct) are those which schedule the XMIT transmission.

FIGURES 40 through 49 illustrate the data FIFO instruction queue initiation and the data storage mechanism.

Utility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
F1	6 XMT CHD 1 - READ	DPU STAT	-16	-17-Lev	8-78-077-	-19-
00050 10091 10000	49432					
40432 40932	#0019 00364 46357					
	00363 #0001 SUB	49358	-0-			
DBI DD STOT I	402241	#9129 SUB 40224	96399			
- pro_kp_aini_i	ne ne	eference Da	ta —			
Format :Decim	al Offline	Range	: 1			

Figure 40 – Segment 3 Network 11 – Read DPU Status Information Or FIFO Instruction Load.



Figure 41 – Segment 3 Network 12 – Read DPU Metering Information Or FIFO Instruction Load.

Utility 1 CDEMO_5	Elements Edit	Go/Srch	Network PD	Refs 17-Lew	Tools 8-re-orr-	Quit P9
Sep. 3 113 1 38 00352 10003 10000 308 40432 00313 00309	1 2017 CHD 3 - 920 F 40432 40397 FETN 0019 1 0019 1 00303 00019 1 00303 00019 1 00303 00019 1 0019 1 0019 1 0019 1 0019 1 0 0 0 0 0 0 0 0 0 0 0 0 0	49358	LIES			
DPU_READ_PWR_3	1500 40224	#9283 (SUB 40224 ference Dat	10382			
Format :Decima	1 Offline	Range	1			

Figure 42 – Segment 3 Network 13 – Read DPU Power Information Or FIFO Instruction Load.



Figure 43 – Segment 3 Network 14 – Read DPU Breaker Status Information Or FIFO Instruction Load.



Figure 44 – Segment 3 Network 15 – Read DPU Status Information Or FIFO Instruction Load.

Utility	Elen	ents Edit	Ga/Srch	Network	Refs	Tools	Quit
Seg. 3 a	16 1 41 XHT C	ND 6 - READ	PCD STATUS	10	-r/-Lev (-ro-urr-	-0
00355	10005 40432						
	10000 40397 ISUB 1718						
⁰	10132 #0019						
00313	66393 09364	40357					
	00303	10002	40350				
		SUB -	- I -	-()-			
		10224	19129	90385			
DOD. DD	enomic all		4922.4				
- rcs_nu_	31H103_6	Be	ference Da	ta —			
							- 1
Fornat	:Decinal	Offline	Range	1			

Figure 45 – Segment 3 Network 16 – Read PCD Status Information Or FIFO Instruction Load.



Figure 46 – Segment 3 Network 11 – Read PCD Metering Information Or FIFO Instruction Load.



Figure 47 – Segment 3 Network 18 – Read PCD Power Information Or FIFO Instruction Load.

Utility	Elements Edit	Go/Srch No	twork Refs	Tools B-DB-DFP	Quit
Seg. 3 019 1 44 00359 10009 00359 10009 0000 SUB 40432	49432 49432 1997 1918 1919 1918 190019	PCD STAT 4005	KEI .		
- PC3 BD STAT 9	00307 1037 00383 #8602 SUB - 46224	49358 #9898 SUB 49224	()— 199		
	Be	ference Data			
Format :Decima	ol Offline	Range : 1	ı		

Figure 48 – Segment 3 Network 19 – Read PCD Breaker Status Information Or FIFO Instruction Load.

Utility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
Sey 3 1420 14 00359 10010 100000 10000 100000 10000 10000 10000 10000 10000	5 XHT CHD 10 READ 1 40432 40397 FTH	40358 40958 10905 SUB		- 17-Lev 0	-10-407	-13
PCD_RD_STAT2_	10 B	eference De				
Format :Decin	al Offline	Range	: 1			

Figure 49 – Segment 3 Network 20 – Read PCD Status Information Or FIFO Instruction Load.

SEGMENT 3 NETWORKS 21 THROUGH 30:

As the previous networks 11 through 20 only data access instructions were programmed in the device. Networks 21 through 30 perform control instructions. As illustrated in the DPU 2000R Automation Manual and the PCD 2000 Modbus Protocol documents, the procedure for performing control is to write a group of registers parameterizing the control (usually writing 5 consecutive registers) and then writing one single register with the execute command (usually 1) and send it to the relay within 100 seconds of the parameterization commands. As illustrated in FIGURES 51 through 60, the procedure to do this is shown in FIGURE 50.



Figure 50 – Write Ladder Logic Methodology.

In order to do a write instruction for the DPU, the FIFO must be preloaded with an instruction between 21 through 25 and then the FIFO must be loaded with the trigger instruction (a Write of 1 to register 41154) which is pointer 20. In order to do a write instruction for the DPU, the FIFO must be preloaded with an instruction between 26 through 30 and then the FIFO must be loaded with the trigger instruction (a Write of 1 to register 41154) which is pointer 31. FIGURES 51 - 60 illustrates the ladder logic to perform the base relay control and read data structures by which this entire program is predicated upon.

Utility CDENO 5	Elements Edit	Ga/Srch	Network	Refs	Tools	Quit
Seg. 3 #21 1 40 99360 #0021 #0099 [SUB 40432	6090 TPLP (040 20 10397 1039	-20	#6029 49 #6099 49 SUB F 40432 #9	432 397 IN 019		ŭ
Pornat :Decing	Bernard B	eference Da	ta			

Figure 51 – Segment 3 Network 21- Place DPU Trip Command In FIFO

Utility 21CDEH0_5 Sec. 3 #22 17	Elements Edit	Go/Srch	Network	Refs 17-Lev	Tools 1 FB OFF	Quit
99361 18022	49432		6029 494	132		
#0000 SL/B 40432	40397 FIN		0000 403 SUB F1 0432 100	197 IN		
DPU_CLOSE_2022		200000-200				
8	n	eference Dat	a			8
Fornat :Decina	1 Offline	Range :	1			

Figure 52 – Segment 3 Network 22 - Place DPU Close Command In FIFO

Utility	Elements	Edit	Go/Srch	Network	Refs	Tools	Quit
Sey. 3 123 1 4 00562 10023 10000 3000 300 40432	B DPU HESET	TARGETS	(20 - 23)	100020 40 #0000 40 8080 P 10432 #9	4132 	0-10-UTT-	-13
C DPU_RST_TGT_2	023	- Bet	ference Da	ta —			
- Format :Decim	s] 0f1	line	Bance	: 1			

Figure 53 – Segment 3 Network 23 - Place DPU Reset Targets Command In FIFO

Utility	Elenents	Edit	Ga/Srch	Network	Refs	Too 1s	Quit
Sey. 3 1624 1 47 00563 10024 10000 SUB 16432	9 DPU NESET 40432 40397 40397 PIN 90319	ALABHS	20 - 24)	#0020 90 #0000 90 SUB 10132 #0	432 397 IN 019	0-10-011-	Ð
DPU_RST_ALMS_	2024	Bef	erence Da	ta —			
. Format - Docing		line	Barce	- 1			

Figure 54 – Segment 3 Network 24 - Place DPU Reset Alarms Command In FIFO

Utility	Elements	Edit	Ga/Srch	Network	licefs	Teels	Quit
Seg. 3 #25 1 5	O DPU RESET	BLT STAT	€ 20 -25	0			11 A
00364 #0025	40432			10020 40	432		
40000	40397			10000 40	397		
SUB 46432-	PIN -			SUB P	IN		
[<u></u>							
÷							
DPIL BST REV S	TOT 2025						
- Mojnarjacija	ini_coco	- Ref	erence Da	ita —			
							1
Format (Bearing	an	line	Dancia	- 1			
Format :Decim	al 001	line	Range	: 1			

Figure 55 – Segment 3 Network 25 - Place DPU Reset Status Command In FIFO

Utility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
Bey. 3 126 1 5 33365 1 80026 80000 [SUB 40432]	1 PCD TRIP (26-31) 49432 60397 FUN 80019		10 10000 40 15UB F 40432 #0	432 397 1N 019	0-10-WII-	-12
PCD_TRIP_20_2	6 Te	ference Ba	ta —			
Format :Decim	al Offline	Bance	: 1			

Figure 56 – Segment 3 Network 26 - Place PCD Breaker Trip Command In FIFO

Jtility	Elements Edi	t Go/Srch	Network	Refs	Too 1s	Quit
Bey. 3 1227 1 5 30366 #0027 10000 318 40432	2 PCB CLASE (27 40432 40397 FTN #0015	-31)	#0031 49 #0000 40 SUB 40432 #0	4132 1997 11N - 1019	0-10-UTT-	-12
PCD_CLOSE_20_	27	- Reference D	ata —			
Format : Becin	a) Offin	e Barge	- 1			

Figure 57 – Segment 3 Network 27- Place PCD Close Command In FIFO

2000 5 Sey, 3 028 1 53 00367 0000 SUB 40432	Elements Edit 13 14 14 14 1	Go/Sirch 15 (28 - 31)	Network P 10 4943 0000 4035 SUB 9031 0432 9035	efs 7-Lev 8-1 2 7 9	tools B- <mark>UTT</mark>	Quit P3
PCB_RST_TGT_20	28]	Range :	a			

Figure 58 – Segment 3 Network 28 - Place PCD Reset Targets Command In FIFO

Utility	Elenents	Edit	Go/Srch	Network	Refs	Tools	Quit
Bey. 3 829 1 5 99369 H0029 80000 308 40432	49432 40397 FIN #0019	ALARMS	(29 -31)	100031 49 100090 49 5UB F	432 397 1N 019	0-ro-urr-	-12
PCD_RST_ALMS20	629 	Be	ference be	ita —			
- Format :Decim	s1 001	fline	Bange	: 1			

Figure 59 – Segment 3 Network 29 - Place PCD Reset Alarms Command In FIFO

Utility	Elements Edit	Go/Srch Ne	twork Refs	Tools	Quit
Bey. 3 830 1 55 00559 +0030 80000 SUB 40432	5 PCD RESET STATUS 40432 40397 EIN 0019	(39 - 31) #00 00 50 404	31 40432 00 40397 8 IFIN - 32 #0019		
PCB_RST_STAT2	230]Te	ference Data			

Figure 60 – Segment 3 Network 30 - Place PCD Reset Status Command In FIFO

Segment 4 Network 1: Operator Interface Control Screens

In this example, the PLC program exists as a central data concentrator. In this case, the program was developed to have a register be set in order to trigger the control instructions via an operator interface. The MMI control screens are described herein on a network to network basis.

Register 40051 is the input bit control register (the MAGELIS sets the bit momentarily) and the ladder logic fills the FIFO with the appropriate command for toggling the graphic. Bit 16 or 14 in the word is set to indicate that automatic or manual control for restoration is followed. Automatic restoration allows the logic for restoration to be enacted. If the Manual control is selected, the operator via the operator screen controls restoration.

Utility	Elence	nts Edit	Go/Srch	Network	Refs	Tools	Quit
F1 CDE	10_5 13-	F4	-15	-16	-17-Lev B	-F8-0FF	-19-1
Sey. 4 11	1 Se HHL AUTO 0016 ()- 0051 01100 32245 01100 0011 ()- 0014 ()- 0014 ()- 00101 01101 8051 01101) MANUAL CO	NTROL .				
Format :	lecimal	Offline	ference Da Range	ta			

Figure 61 – Segment 4 Network 1- MAGELIS F1 And F2 Function Key Auto Manual Control Logic

SEGMENT 4 NETWORK 2:

This is more MMI control logic required for the MAGELIS operator interface. NOTE the pushbuttons for trip, close and reset operations only operate when the system is in AUTOMATIC mode.

Utility	Elements Edit	Ga/Srch	Network	lefs	Teels	Quit
1 CDENO_5	P3P4	F5	-P6	-17-Lev B	-F8-0FF	
Seg. 5 82 1 57 1	HUTU - MAN LIGHT C	ON THOL				
01200 10015	#0014					
4 -						
46055	40055					
11811	- TISIT -					
40001-	40001-					
01200 #0015	88814					
	400 -					
40055	40055					
10011	HEEG1					
	00000					
" MMI_STAT_MAM_A		Province De	1			
8	110	a erence pa	ta.			
						Ĩ
Format :Decima	1 Offline	Bange	: 1			

Figure 62 – Segment 4 Network 2 - MAGELIS F1 And F2 Function Key Led Control Auto Manual Control Logic

SEGMENT 4 NETWORK 3:

This network upon the MMI control screen being issues a system reset, the pending control operations, buffers and latched commands are reset to an initial state.

Utility	Elenents E	lit	Go/Srch	Network	licits	Tools	Quit
Bey. 4 #3 1 58 #0012 40051 32215 #0091	Peset Process 01000 01900 48397 40397 40397 40397 40397 40397 40397 40397	40143 40143 X0R 40919		-7D.	-f7-L8¥ 0	-7 0- <mark>UT7</mark>	
		— Refe	rence Da	ta —			
- Format :Decim	al Officia	ine	Bange	: 1			

Figure 63 – segment 4 network 3 - system reset logic

SEGMENT 4 NETWORK 4:

If the control key for a MANUAL TRIP of the DPU is depressed on the MMI, this logic construct loads the FIFO with the XMIT pointer commands 21,20 to perform a breaker trip operation on the DPU 2000R. Bit 15 of register 40051 is set by the MMI to trigger this instruction (SENS). The ladder logic is illustrated in FIGURE 64.

Utility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
Seg. 4 #4 1 59	TRIP DPU 20008	-15	-ro	-17(-164 0	-10-0111	Ω
40051 SENS -	01200 00360					
	01200					
No Symbol/Desci	riptor available		22			
	Net	erence Da	ta —			1
Format :Decim	al Offline	Range	: 1			

Figure 64 – Segment 4 Network 4 - MAGELIS Pushbutton Manual Trip Logic

SEGMENT 4 NETWORK 5:

If the control key for a MANUAL CLOSE of the DPU is depressed on the MMI, this logic construct loads the FIFO with the XMIT pointer commands 22,20 to perform a breaker trip operation on the DPU 2000R. Bit 13 of register 40051 is set by the MMI to trigger this instruction (SENS). The ladder Logic is illustrated in FIGURE 65.

Utility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
Seg. 4 85 1 60	CLUSE dpu BREARER	19	-10-	-rr-bev o		-0
10013						
90051 - SENS	01200 00351					
#9001						
lí í	91209					
"No Synbol/Desci	riptor available Bef	erence Da	ta —			
Format :Decina	1 Offline	Range	: 1			

Figure 65 – Segment 4 Network 5 - MAGELIS Manual Close Pushbutton Logic

SEGMENT 4 NETWORK 6:

If the control key for a MANUAL TRIP of the PCD is depressed on the MMI, this logic construct loads the FIFO with the XMIT pointer commands 26,31 to perform a breaker trip operation on the DPU 2000R. Bit 11 of register 40051 is set by the MMI to trigger this instruction (SENS).

Itility	Elements	Edit	Go/Srch	Network	Refs	Tools	Quit
Seg. 4 16 1 61	TRIP PCD B	-F4 REAKEIR	-rs	-P6	-87-Lev 8	-re-orr-	-19
19011)—				
90051 - SENS	0120	00 0035					
#0001.	912	∋9					
No Synbol/Desci	riptor avai	lable					
		- Ret	ference Da	ta ——			1
Format :Decima	1 00	Fline	Range	: 1			

Figure 66 – Segment 4 Network 6 - MAGELIS PCD Manual Trip Pushbutton Logic

SEGMENT 4 NETWORK 7:

If the control key for a MANUAL CLOSE of the PCD is depressed on the MMI, this logic construct loads the FIFO with the XMIT pointer commands 27,31 to perform a breaker trip operation on the DPU 2000R. Bit 5 of register 40051 is set by the MMI to trigger this instruction (SENS).

Utility	Elements Edit	Ga/Srch	Network	Refs	Tools	Quit
Seg. 4 87 1 62	CLOSE PCD BREAKER	19	- 10		-ro-urr-	-0
-						
)—				
49651	91209 60366	50 C				
#9661						
lt '	01200					
-						
the Synbol/Descr	iptor available	lavance De	-			
			ta.			
						Ĩ
Parent (Barles	1 00011-00	Bancos				
FORMAC SPECING	a ournee	nange	1			

Figure 67 – Segment 4 Network 7- MAGELIS PCD Manual Close Pushbutton Logic

SEGMENT 4 NETWORK 8:

If the control key for a MANUAL TRIP of the TPU is depressed on the MMI, this logic construct loads the FIFO with the MSTR pointer commands 7,6 to perform a breaker trip operation on the DPU 2000R. Bit 11 of register 40051 is set by the MMI to trigger this instruction (SENS). Note this operation sends a Modbus Plus command to the TPU.

Utility	Elements I	Edit	Go/Srch	Network	Refs	Tools	Quit
1 20090_5 Sey_ 4 #8 1 63 1 20005 90051 -SENS - 20001		P4()- 0 00145	-	16	-77-Lew 8	n <mark>un</mark>	19
Na Synbol/Descr	9120 iptor availa	abic		12			
Format :Decima	1 066	— Here	Range	ta : 1			

Figure 68 – Segment 4 Network 8 - MAGELIS TPU Manual Trip Pushbutton Logic

SEGMENT 4 NETWORK 9:

The MAGELIS operator interface does not display Floating Point Values. All the mathematics in this program is performed using floating point math. In order to display the information on the MMI display (MAGELIS), it must be converted from floating point to integer for display, Kwatts for phases A, B, C, and loading of the DPU prior to the TPU trip. These values are calculated using floating point math instructions.

Dtility Fl COEND 5 Sey. 4 #9 1 64	Elements Edit 13 Pd magelis-ku display	Go/Sech PS	Network 16	Refs 17-Lev B	Tools Room	Quit
41739 41122 1911 01071 41747 41128 1911 01071 01071	41741 41324 41324 41327 41305 41105 41130 41130 41130 41130	41743 41126 2MTH CHUP1				
	fie	ference Ba	ta			

Figure 69 – Segment 4 Network 9 - MAGELIS Watt Hour Display In Integer Units

SEGMENT 4 NETWORK 10,11,12:

The operator is also able to reset the target information via the MAGELIS MMI. If the unit is in manual mode, the operator may depress the function key to reset the targets on the TPU (BIT 8 REGISTER 40051) DPU (BIT 10 REGISTER 40051) AND PCD (BIT 6 REGISTER 40051). The ladder logic for these constructs are listed in FIGURES 70 through 72.

P3 P4	-15	-F6	State Land L	100 0000	1000
0140 01200 0015 01200 0015					-12
ptor evailable Ref	ference Da	te			
	ptor available 0ffline	ptor awilable Offline Bange	ptor evailable Offline Bange : 1	ptor avoilable 00148 01200 0148 01200 0148 01200 0148	to target rest 00146 01200 00147 01200 00148 01200 ptor evailable Beference Bata 0fflise Bange : 1

Figure 70 – Segment 4 Network 10 - MAGELIS TPU Manual Trip Pushbutton Logic

Utility	Elements Edit	60/Sech	Network	Refs	Tools	Quit
1 COEMO 5	-13	-15	-F6	-17-Lev 8	-P8-011-	-19
Seg. 4 #11 1 66	dug target reset					
	-0					
80010	00362					
90951	01200 00363	1				
H SEMS -	L_()					
\$9991 ¹	66354					
	01200					
lt i						
Ho spieotzeescri	ptor available					
	ner	erence pa				
						-
Format (Decimal	Offline	Bange	: 1			
Format (Decimal	Offline	Bange	: 1			

Figure 71 – Segment 4 Network 11 - MEGELIS TPU Target Reset Pushbutton Logic

Otility	Elements Edit	Go/Sech	Network	Refs	Tools	Quit
Seg. 4 812 1 67	pod target reset	-10	-ro	-ev-Lev b	-ra-um-	-19
Louis I	Laware C.					
303001		_				
90951	01200 00368					
#9961	00365	-				
	01200					
-						
Ho Sueho Labersce	istor emilable-					
	Ref	erence Da	ta —			i
Fornat (Decina)	1 Offilie	Bange	: 1			

Figure 72 – Segment 4 Network 12 - MAGELIS PCD Manual Target Reset Pushbutton Logic

SEGMENT 4 NETWORKS 13 AND 14:

The MMI displays data via bit data which toggles the graphics. The logic constructs in Networks 13 and 14 illustrate the logic to indicate on the display the breaker status of the TPU as well as the AUTO/MANUAL PLC program control. The logic is illustrated in FIGURES 73 and 74.

ility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
01201 E 01201 EC016 91011 91011 91011 91011 91011 91011 91011 91011 91011 91011 91011 91011 91015 91011 91015 91011 91010 910 9101 910 910 910 910 910 910	1 tju breaker status 01201 - - - -	10016 41011 HBIT 80001 10015 41011 HBIT 80001		-77-Leu	8-78-07	-12
TRU_S2A	Ref	erence De	ita —			
Format (Dec ins	a orrine	Banac	- 1			

Figure 73 – Segment 4 Network 13 - MAGELIS PCD Breaker Status Logic To Manipulate The Screen Graphics.

Utility	Elements Edit	60/Srch	Network	Refs	Tools	Quit
Sey. 4 #14 1 65	9 magelis autorm	amoni atatea	10	-ev-Lev c	-10-011-	-13
01200 00014		0013				
41011 /811 0001		41011 10011 00001				
01200 10013		10014				
#0001		10001 #0001				
mm)_Stat_man_e	NUTO	Reference Ro	ta			
E Format (Decine	al Offline	Bange	T 1			

Figure 74 – Segment 4 Network 12 - MAGELIS Auto/Manual Screen Status Icon Logic

Segments 5 and 6 performs the logic which initiates the procedure upon a TPU monitored/protected feeder trip. The explanation of the logic follows.

SEGMENT 5 NETWORK 1:

Since 52a and 52b are not direct points within the TPU, the PLC program reads WINDING currents for phase A (41702), B (41704), and C (41706) and if the currents are less than 2 amperes, the TPU denotes the relay as tripped and generated 52a (01201) and 52b (01202) internal status coils. Note that labels have been affixed to each of the registers contacts and coils. The logic is illustrated in FIGURE 75.



Figure 75 – Segment 5 Network 1 - Calculate 52A And 52B On TPU Since Contacts Are Not Mapped.

SEGMENT 5 NETWORKS 2, 3, 4, And 5:

Segments 2, 3, 4, and 5 (for the sake of this program since it is a demonstration and illustration of the power of the relay and PLC's capabilties), convert the KW of Phase A, B, and C, which was read from the TPU and supplied to the feeder (controlled by the PCD). The Compact 984 PLC only performs integer math on numbers from 0000 to 9999. The PLC calls a subroutine to convert the number from a 32 bit number integer (which is obtained via the MSTR block and stored in registers 41728 and 41729 [Phase A integer Units], 41730 and 41731 [Phase B Integer Units] and, 41732 and 41733 [Phase C Integer Units]) and converted into floating point numbers which enable easy mathematical conversion feeder load control. The floating point converted numbers are calculated in the subroutine segment (segment 7) and are labeled as JSR 2 and JSR 1. The floating point numbers are located in registers 41739 and 41740 [Phase A Floating Point quantity]], 41741 and 41742 [Phase B Floating Point quantity], and 41743 and 41744 [Phase C Floating Point quantity]. Since this program was tested on a simulator, the values were made to be positive quantities for the sake of illustration in a demonstration environment.

Network 5 adds each of the quantities and stores it for comparison to a predefined feeder supply value which is compared when the line sectionalizing occurs.

Utility 71CDEH0_5	Elenenta	Edit	Go/Srch	Network	Refs Refs	Tools 8-16-011	Quit
Seg. 5 12 7 71	CALCULATE 41728 413 41300 413 BL3M 18 #0001 800	RNA AND IF 727 #0992 J381 01 #0901	41351 41739 80.8M 80602	11739 0 41100 80.02	11302 4110 4110 4110 18M CHS	09 41192 	-
* 1PU_526		Refe	rence Da	ta —			
- Format :Decim	a1 0i	fline	Range	: 1			

Figure 76 – Segment 5 Network 2 - Calculate KW For Phase A

Utility 1 CDEMO_5 Sey. 5 03 1 77	Elements Edit 13 Pd 2 CALC PHASE B RM IF	Ga/Srch Network R PS PG P NES NAKE POS	fs Tools Quit - <mark>Lev 6-78-077</mark> -79					
01201 00163	41730 41729 #000 338 41300 41301 #000 8L2m #0961 #0601	2 41351 41741 01300 11 41741 41100 BL2H BL2H BL2H BL2H BL2H	41100 41102 4100 41241 1877H - BLKR CHSIN 80002					
TPU_524	TPU_524							
Format :Decir	nal Offline	Bange : 1						

Figure 77 – Segment 5 Network 3 - Calculate KW For Phase B

Utility 1CDEH0_5 Sec. 5 #1 73	Elements I CALCULATE P	41it Go∕Si 4 PS CKJ - IF N	Ch Networ Pô G MK PS	rk Refs 17 Lev	Tools 8-re-Orr	Quit 19
01201 20163	41232 41731 41300 41303 BLAM BLAM BLAM	10002 4139 1058 10001 4129 10001 8129 10001	1 41743 3 41100 1 BLEM 2 #0002	01392 411 411 127 CHS	09 41192 09 41743 TH BLRH TH 80092	01103
TPU_526		- Beference	Data —			
- Format :Decima	പാണ	ine Ra	ge : 1 —			

Figure 78 – Segment 5 Network 4 - Calculate KW For Phase C

Utility	Elements Edit	Go/Srch	Network	licfs	Tools	Quit
Seg. 5 45 1 74	CALULATE TPU 3 PHAS	E PUR	-10-	-rr-Lev o	-re-urr-	-13
01103 41241	41239 41243 41105	Г				
	H H					
41101 IBL KN	41101 41103 41745 - JENTH - JENTH - JBLKM					
#6082	ADDET ADDEP #0002	1				
4No Symbol/Descr	iptor available	erence Da	4			
Format :Decina	1 Offline	Bance	- 1			

Figure 79 – Segment 5 Network 5 - Calculate KW For All Three Phases

SEGMENT 5 NETWORK 6:

Since the TPU does not have 52a and 52 b reported for a trip condition (since it is not wired into the simulator in this example), if the current of each of the phases is a value less than 2 amps, the TPU is determined to be tripped. This instruction construct sends a trip command (via the commands 6 and 7) via the FIFO for the MSTR block. This trips the TPU to ensure the state of the unit. The network logic is illustrated as per FIGURE 3 of this note. This network performs the action in MANUAL mode.



Figure 80 – Segment 5 Network 6 - Trip TPU If Readings Are Less Than 1 A Per Phase (Since 52A And B Contacts Are Not Wired Into Demo Case)

SEGMENT 6 NETWORK 1:

This network (although out of place in the scheme of things), takes a pushbutton input from the Magelis MMI and places the PLC program in the MANUAL or AUTOMATIC restoration status. If coil 01200 is a energized, the program is in AUTO mode. If the coil 01200 is de-energized, the program is in manual mode. The logic is illustrated in FIGURE 81.

Utility	Elements Edit	Go/Srch	Network	Refs	Too 1s	Quit
Beg. 6 11 76 01101 01102 01100 01102 01200	AUTO DR MANUAL COM		-10	-17-Lov 8	-19-011	
Forest :Decis		ference Da	ta			

Figure 81 – Segment 6 Network 1- Upon MMI MAGELIS Action, Place The Program In Manual Or Automatic Restoration Mode.

SEGMENT 6 NETWORK 2:

This network checks the TPU TARGET status which was stored in register 41725. If a target is on the front panel interface, an indication is given by coil 001150 which is used in this program. The logic is illustrated in FIGURE 82.



Figure 82 – Segment 5 Network 6 - Trip TPU If Readings Are Less Than 1 A Per Phase (Since 52A And B Contacts Are Not Wired Into Demo Case)

SEGMENT 6 NETWORK 3:

Since the TPU does not have 52a and 52 b reported for a trip condition (since it is not wired into the simulator in this example), if the current of each of the phases is a value less than 2 amps, the TPU is determined to be tripped. This instruction construct sends a trip command (via the commands 6 and 7) via the FIFO for the MSTR block. This trips the TPU to ensure the state of the unit. The network logic is illustrated in section 82. This network performs the action in AUTOMATIC mode. The coil 01151 carries this action to the next instruction network.

Utility	Elements Edit	Go/Srch Network	licefs	Tools	Quit
Sey. 6 #3 1 7	S TPU TRIP BREAKER	10	- LOW		- A2
01150 01200	#0007 40224	#0006 40224 0	1151		
	H0000 40543	40000			
	SUB FIN -	SUB - PIN -			
11	49224 46619	492241 #60191			
TPU TABGET A	UTUITEU HAS TABGET D	ето			
	lie lie	ference Data			- 1
					1
Format :Beci	nal Offline	Range : 1			

Figure 83 – Segment 5 Network 6 - Trip TPU If Readings Are Less Than 1 A Per Phase (Since 52A And B Contacts Are Not Wired Into Demo Case)

SEGMENT 6 NETWORK 4:

If there is no fault, calculate the loading prior to the trip of the TPU. This figure is used to determine if the DPU at the other end of the feeder has the capability to drive the load of the PCD 2000. The ladder logic is illustrated in FIGURE 84 which follows.

Itility	Elements Edit	Ga/Srch	Network	Refs	Teels	Quit
Ser. 6 #4 1 79	NO TPU TRIP - GE	T BU UNLUES	-10-	-17-684 (e-re-urr-	-12
01200 01201	41	783				
	41	745				
	12	nth -				
	nt	DIF				
"MMI_STAT_MAN_A	010					
		Reference Da	ita —			1
Format :Decima	1 Offline	Bange	: 1			

Figure 84 – If No TPU Trip Calculate KW Values Prior To Trip For Later Loading Calculations For Bus Line Sectionalizing Calculations

SEGMENT 6 NETWORKS 5, 6, 7, 8, 9, AND 10:

If the loading is appropriate for the DPU to supply the PCD circuit in lieu of the TPU which tripped, the following sequence occurs.

The DPU status is checked and the breaker is closed as long as the TPU 2000R breaker is tripped.

The program is delayed by 3 seconds and the PCD 2000 is then closed and the close is verified by the program.

The operator interface echo's the state of the restoration sequence on the operator interface as each of the steps is being performed.

Utility	Elements E	dit	60/Srch	Network.	Refs	Tools	Quit
Seg. 6 #5 1 80	FJ DPU BREAKER	1 IN 7 CU	USE PC07	-16	-17-Lev 8	10-011	-19
P 01150 01200	#0001 41798 41798 41798 90001	#0001 41798 5EMS #0001 01104 41850 41247 41247 41247 CHPPP					
		- Ref	erence Da	ta —			
Formed - Base Law	1 8771	5000		· *			

The ladder logic networks are illustrated below as figures 85 through 87.

Figure 85 – Segment 6 Network 5 – Check DPU Breaker Status

CDEHD 5 Seg. 6 85 8 01115 01105	Elements Edit 1 PCD CLOSE - RESTOR 00027 90432 100900 9037 10091 90019	GovSrch Network Refs Tools Quit F5 F6 F7 - E00 8 - F8 - 077 - F9 12 FEEDER 00031 40432 01106 01006 10032 F1 - 0100 01006 0019 - 0100
01115	[P] 01105	01113
No Symbol/Des	criptor available Re	ference Bota
- Fornat :: Dec i	nal: Offline	Bange : 1

Figure 86 - Segment 6 Network 6 – Close PCD In Anticipation Of Feeder Restoration Upon TPU Trip

Dtility	Elements Edit	60/Srch	Network	Refs	Tools	Quit
71 00270 5 Seg. 6 17 162 01106 01000 01108	2 UAIT 3 SECONDS FOR 01107 01106 1.0 1.0 1.0 1.0 1.0	12 HEPLY 889	-F6 : TRP () 91197	F7-Lev	<u>. 10 01</u> -	19
BESTORE_PCD_B	REAKER	ference Be	ita ———			
Fornat :Decin	al: Offline	Bange	; 1			

Figure 87 - Segment 6 Network 7 - Wait 3 Seconds For Breaker Action

Utility	Elements Edit	Ga/Srch	Network	Refs	Tools	Quit
Sey. 6 #8 1	B CHECK TO DETERMINE	IF PCD CLI	ISED	- LOW	0-ro-0rr-	- * *
01107	10009 10009 10000 10032 100432 100432 100432	01111	21000 01	()— 112		
PCD_CHK_BRK	R Be	ference Bat	la —			
Fornat :Dec:	imal Offline	Range	: 1			

Figure 88 - Segment 6 Network 8 - Check To Determine If PCD Is Closed

Itility	Elements Edit	Go/Srch 15	Network P6	Refs 17-Lev	Tools 8-re-orr-	Quit.
		90638 357 002 224	40358 #0898 01 SUB 16224	0— 111		
No Synbol/Desc	riptor available	D-2	72			
- Format : Becil	a) Offline	Bance	- 1			

Figure 89 - Segment 6 Network 9 - Wait For PCD Response To Breaker Action

Utility	Elements	Edit	Go/Srch	Network	Refs	Tools	Quit
2 - 2020/85 Sey. 6 #10 1 85 01111 #00001 11047 5285 #0001		VERIFY	PCD SZA	ΨD.	-17-Lav 8	- 10 - UT	-13
		Be	sference Da	ta ——			
- Format :Decima	1 OF	fline	Bange	: 1			

Figure 90 - Segment 6 Network 10 - Verify That Breaker Is Closed.

NOTE this program was developed for a demonstration of line restoration/sectionalizing applications. The TPU simulator used did not have breaker status, thus the need for the additional logic to calculate and maintain the correct status of the TPU breaker action (even if a manual trip command from the front panel was performed, the status of 52A and52B derived from this program is valid).

Subroutines

Two subroutines are included in this program. The subroutines are called from within the main program located in Segments 1 through 6 (JSR 2) and from within the subroutine (JSR 1). The subroutines are:

SUBROUTINE 1 – Convert an UNSIGNED 32 bit double register integer into a floating point number.

INPUT INTEGER to be converted: 41300 and 41301

FLOATING POINT RESULT located in 41351 and 41352.

SUBROUTINE 2 – Convert a SIGNED 32 bit double register integer into an absolute value floating point number.

INPUT INTEGER 41300 and 41301

NORMALIZED FLOATING POINT NUMBER 41330 and 40331.

These subroutines require constants to be placed in specific registers as illustrated in the constant screen windows listed at the end of this document. The constant values are used in allowing the subroutine to calculate the numbers correctly. NOTE: these subroutines are required for three reasons:

- The TPU,DPU and PCD use true integer numbers and the PLC only calculates numbers using integer math for a range of 0000 to 9999 (Compact 984 limitation).
- The COMPACT 984 PLC can perform mathematics calculations in IEEE Floating POINT, thus a calculation must be made from the PLC numbers (0000 to 9999 or 00000000 to 999999999 [double precision integer]) to floating point numbers.
- The MAGELIS MMI cannot display IEEE floating point numbers, so the results of the floating point number must be changed to the integer format required by the MMI.

SEGMENT 7, the last segment in the program, is not set up in the ladder logic segment scheduler (as is necessary for ladder logic subroutines). As illustrated in the ladder logic segments, 1 through 9 (FIGURES 91 through 96), the subroutine starts with a LAB instruction and ends at the RET command. The ladder logic segments are listed with the constants required for operation.

Utility	Elements Edit	Go/Srch	Network	Refs	Tools	Quit
21 - 20200 5 Sey 2 M 1 86 10001	P3 P4 32 BIT UNSIGNED TO	PP NUMBER	rb	-77-Lav 8	re- <u>orr</u>	n
No Symbol/Descr	iptor available Be	ference Da	ta			

Figure 91 - Segment 7 Network 1 - 32 Bit Integer To Floating Point Number . Subroutine 1

Utility	Elements Edit	Go/Srch N	ctwork Refs	Tools Q	lit
1 90370 5 Sey. 7 #2 1 87 41309 81399 81399 81399 41398 41398 11398	1302 41309 41309 41309 41309 41309 4400 84309 4400 84309 41306 41303 41312 41309 41312 41309 9001 11 41312 41309 9001 10 9011 10001	1389 41309 41309 18807 80001 899 907 907	41309 41309 41309 41309 41309 41309 41309 41309 41309 41309 1 80001	8-P8-077-P 11309 11309 11309 11309 001 11309 0 11309 1130 11309 1130 1	-()
- Format :Decir	al Offline	Range :	1		

Figure 92 - Segment 7 Network 2 - 32 Bit Integer To Floating Point Number . Subroutine 1

tility	Elenents	Edit	Go/Srch	Network	Refs	Tools	Quit
1	_r3	_r1	-rs	-76	-17-Lev 8	-re-orr-	-r9
01300	11309	11398		41322	4131	6	
	41309 -BRDT #0001	41318 HENTH CNUTP	F	41314 EMTH ADDEP	4132 BLR #000	4 H 2	
	11309	41304	F				
	41309 BROT #0001	ENTH HULFP	F				
No Symbol/Desci	riptor avai	ilable Bef	erence De				
Format :Decima	1 06	fline	Range	: 1			

Figure 93 - Segment 7 Network 3 -32 Bit Integer To Floating Point Number . Subroutine 1

Utility	Elements Edit	Go/Srch	Network Refs	Tools Quit
CDEHO_5		-rs	-P6	8-F8-0FFF9
Seg. 7 #4 1 89				
91300 11391	11302 11301	41389	41309	41399 01301
41309	41309 41309	41309	41309	41309
BL.KM #0001	AMD BLRH #0001 #0001	B801 #0001	BR07 #0001	[BR07] #0001
11308	11366 11303 1130	9	11309	11399
41398	41312 41309 4139	9	11309	11399
41398	CNUIF #6601 #099	1	#0961	#0991
Mo Symbol/Descr	iptor available Re	ference Da	ta	
L Format :Decima	1 Offline	Range	: 1	

Figure 94 - Segment 7 Network 4 - 32 Bit Integer To Floating Point Number. Subroutine 1

Utility	Elenents	Edit	Go/Srch	Network	Refs	Tools	Quit
Sey. 7 #5 1 90	-13-	-14	-10	-10-	-ry-Lev	8-ns-urr-	-12
01301	11309	11398		41322 41	316		
	41309 BROT	41318 - ENTH	-	41314 41 EPITH E	326 MTH -		
	11309	11394	Ē	11	324		
	41369 BROT	41320 ENTH	_	41	328 917H		
		THE P					
Ma Synbol/Descr	iptor avai	lable Bef	erence De	ita —			
Format :Decima	1 00	fline	Range	: 1			

Figure 95 - Segment 7 Network 5 - 32 Bit Integer To Floating Point Number. Subroutine 1



Figure 96 - Segment 7 Network 6 - 32 Bit Integer To Floating Point Number. Subroutine 1

Subroutine 2 uses subroutine 1 and it takes a negative number and converts it to a positive number (used for the sake of this demo to vary the KW readings using those from the simulator). This is used because the simulators use a single phase source and makes KW readings appear negative on some of the phases.

Elenes	ts Edit	6a/Sech	Network	Ref s	Tools	Quit
SIGNED 3	Z BIT TO	FP NUMBER	-rs	-17-Lev	a-ra-orr-	-19
riptor aw	ailable—					
		eference De	te			
	Flores 13 SIGNED 3	Fienests Mit F3 74 SIGNED 32 BIT TO	Elements Edit GavSrch F3 F4 F5 SIGNED 32 BIT TO FF NUMBER	Figurests Edit Ga/Srch Network F3 F4 F3 F6 SIGNED 32 BIT TO FF NUMBER riptor available Reference Data	Flements Edit Go/Srch Network Refs F3 F4 F5 F5 F5 F7 Lcg SIGNED 32 BIT TO FF MUMBER riptor available Reference Data	Figure available Beference Data

Figure 97 - Segment 7 Network 7 - 32 Bit Signed Integer To Floating Point Number. Subroutine 2



Figure 98 - Segment 7 Network 8 - 32 Bit Signed Integer To Floating Point Number. Subroutine 2



Figure 99 - Segment 7 Network 9 - 32 Bit Signed Integer To Floating Point Number. Subroutine 2

PLC Program Constants

As illustrated previously, there are certain constants in 4X memory and 6x memory which must be preloaded into PLC memory for this program to function properly. The screens which follow illustrate the contents of each of the registers which are needed for this program's proper operation.

Utility	Format	Setting	Chylindu	Transfer	Template Disa	ble	Quit
CDENO_5	-13	ř4— liet	ference Dat	a	-17-Lov 8-16-(JFF-	-F9
600500	256	Dec	61050	8	3	Dec	
600501	355	Dec	61050	1	1	Dec	
600502	5	Dec	61050	Ζ.		Dec	
600503	2000	Dec	61050	3	129	Dec	
699504	G	Dec	61050	1	1750	Dec	
600505	10	Dec					
699586	10	Dec					
699567	0	Dec					
699510	256	Dec	61053	0	3	Dec	
600511	355	Dec	61053	1	26	Dec	
600512	5	Dec	61053	2	1	Dec	
600513	2000	Dec	61053	3	257	Dec	
600514	0	Dec	61053	4	1751	Bec	
600515	10	Dec	1000				
600516	10	Dec					
600517	G	Dec					
600518	0	Dec					
600520	256	Dec	61056	0	3	Dec	
699521	355	Dec	61056	1	16	Dec	
600522	5	Dec	61056	2	1	Dec	
Format (Decina)	000	line	Bange :	1			

Utility	Format	Setting	Chylindu	Transfer	Template Disc	ble	Quit
CDENO_5	-13	F4— Ref	ference Dat	ta —	-17-Lev 8-16-0	JFF —	-F9
600523	2660	Dec	6105	53	283	Dec	
600524	.0	Dec	6105	i4	1777	Dec	
600525	10	Dec					
600526	10	Dec	6105	30	3	Dec	
600527	. 0	Dec	6105	31	4	Dec	
600528	0	Dec	6105	52	1	Dec	
			6105	33	898	Dec	
600530	256	Dec	6105	24	1793	Dec	
600531	355	Dec	6105	35	0	Dec	
600532	5	Dec					
600533	2000	Dec					
600534	0	Dec					1
600535	10	Dec	6105	20	3	Dec	
600536	10	Dec	6106	21	2	Dec	
600537	6	Dec	6106	7Z	1	Dec	
600538	Ó	Dec	6105	23	905	Dec	
600539	0	Dec	6106	24	1798	Dec	
(11) (11) (11) (11) (11) (11) (11) (11)			6106	5	0	Dec	
Fornat (Decina)	i ore	line	Bange	1			

Utility	Format	Setting	Chylindu Th	cansfer	Template Disa	ble	Quit
CDENU_5	-r3	F4— Ref	erence Data		-17-Lov 8-16-(JFF—	-19-1
600700	256	Dec	611160		16	Dec	
600701	355	Dec	611101		1	Dec	
600702	5	Dec	611102			Dec	
600703	2000	Dec	611103		1154	Dec	
699764	0	Dec	611104		360	Dec	
600705	10	Dec	611105		1	Dec	
699786	10	Dec					
600707	0	Dec					
600708	0	Dec	611130		0010	Hex	
			611131		5	Dec	
600710	256	Dec	611132		1	Dec	
600711	355	Dec	611133		1155	Dec	1
600712	5	Dec	611134		360	Dec	
699713	2660	Dec	611135		2920	Hex	
600714	0	Dec	611136		2926	Hex	
600715	10	Dec	611137		0000	Hex	
699716	10	Dec	611138		0901	Hex	
600717	0	Dec	611139		0001	Hex	
600718	0	Dec	611140		0000	Hex	
100000	900		cause .				
600720	256	Dec	611160		0010	HICK.	
600721	355	Dec .	1611161		0005	nex	
 Format (Decima) 	000	Line	Hange	1 —			

Utility	Format	Setting	Chylindu	Transfer	Template Disc	ble	Quit
F1 CDENO_5	-F3	F4- Ref	erence Da	ta —	-17-Lev 8-F6-(JFF —	-63
600722	5	Dec	6111	62.	1	Dec	
600723	2000	Dec	6111	63	1155	Dec	
699724	. 0	Dec	6111	64	360	Dec	
600725	10	Dec	6111	65	2929	Hex	
600726	10	Dec	6111	66	2020	Hex	
699727	0	Dec	6111	67	0000	Hex	
600728	0	Dec	6111	68	0020	Hex	
			6111	69	0920	Hex	
600730	256	Dec					
600731	355	Dec	6011	90	0010	Hex	
600732	5	Dec	6011	91	0005	Hex	
600733	2000	Dec	6011	92	.0001	Hex	
699734	0	Dec	6011	93	1155	Dec	
600735	10	Dec	6011	94	360	Dec	
600736	10	Dec	6011	95	2020	Hex	
600737	0	Dec	6011	96	2920	Hex	
600738	0	Dec	6011	97	0000	Hex	
			6011	98	9166	Hex	
			6011	99	0100	Hex	
Format (Benins)		line	Bances	- 1			
- rormat - pectral		1102	nange	- 1			

Utility Format Setting ChyWadw Transfer Template Disable Quit

r1	DENO 5	r	4-	Reference Data		8-F8-0	IFF F9
11366	CONU_UAL->	0	Dec	41322		6	Dec
41301	CONU_UAL->	0	Dec	41323		0	Dec
41362	CONST_00FF	255	Dec	41324		6	Dec
11363	CONST FF66	65280	Dec	11325		0	Dec
41304	CONST_25->	0	Dec	41326	COHST_65->	65280	Dec
41365		17280	Dec	41327		18363	Dec
41306		0	Dec	41328		0	Dec
41307		0	Dec	41329		0	Dec
11366		0	Dec	11330	FP_RES_S->	0	Dec
41309		0	Dec	41331		0	Dec
41310		0	Dec	41332		6	Dec
41311		0	Dec	41333		0	Dec
41312		0	Dec	41334		0	Dec
11313		0	Dec	11335		0	Dec
41314		0	Dec	41336		0	Dec
41315		0	Dec	41337		0	Dec
41316		0	Dec	41336		0	Dec
41317		0	Dec	41339		- 0	Dec
11318		0	Dec	11340	constant->	255	Dec
41319		0	Dec	41341	constant->	65280	Dec
41320		0	Dec	41342		831	Dec
41321		0	Dec	41343		0	Dec
L Fornat	: :Decinal	0661	ine	Range : 1			

Utility	Format	Setting	Chylindu	Transf cr	Template Disa	ble	Quit
CDENO_5	-13	P4- Ref	ference Dat	a. —	-17-Lev 8-F6-(IFF-	-F9
600740	256	Dec	61112	0	0010	Hex	
600741	355	Dec	61112	1	0005	Hex	
699742	5	Dec	61112	2	1	Dec	
600743	2000	Dec	61112	3	1155	Dec	
600744	0	Dec	61112	4	360	Dec	
600745	10	Dec	61112	5	292.0	Hex	
600746	10	Dec	61112	6	2020	Hex	
699747	6	Dec	61112	2	9966	Hex	
699748	G	Dec	61112	8	0200	Hex	
			61112	9	0050	Hex	
600750	256	Dec					
600751	355	Dec	61125	0	0010	Hex	
600752		Dec	61125	1	0005	Hex	
600753	2660	Dec	61125	2	0001	Hex	
600754	0	Dec	61125		1155	Dec	
600755	16	Dec	61125	4	360	Dec	
600756	10	Dec	61125	5	2020	Hex	
600757	6	Dec	61125	6	2920	Hex	
600758	G	Dec	61125	7	0060	Hex	
			61125	8	0800	Hex	
600760	256	Dec	61125	9	0380	Hex	
600761	355	Dec					
Foreat (Becina)	0.00	line	Rances :	1			

Utility	Format	Setting	Chylindu	Transfer	Template Disa	ble	Quit
1 CDENO_5	- <u>r</u> 3	ř4— liet	ference Da	ta —	-17-Lev 8-16-(JFF —	-F9
600762	5	Dec	6112	80	0010	Hex	
600763	2000	Dec	6112	81	0005	Hex	
600764	G	Dec	6112	82,	9962	Hex	
600765	10	Dec	6112	83	1155	Dec	
699766	10	Dec	6112	84	360	Dec	
699767	0	Dec	6112	85	2020	Hex	
699768	0	Dec	6112	86	2920	Hex	
			6112	87	0066	Hex	
600770	256	Dec	6112	88	0001	Hex	
600771	355	Dec	6112	89	0001	Hex	
600772	5	Dec					
699773	2660	Dec	6113	10	0010	Hex	
600774	0	Dec	6113	11.	0005	Hex	
699775	10	Dec	6113	12	0002	Hex	
600776	10	Dec	6113	13	1155	Dec	
600777	0	Dec	6113	14	360	Dec	
600778	0	Dec	6113	15	292.0	Hex	
1313200499			6113	16	2020	Hex	
			6113	17	0000	Hex	
			6113	18	0020	Hex	
			6113	19	9920	Hex	
Format (Decina)	i ore	line	Bance	- 1			

Utility Format Setting ChyWadw Transfer Template Disable Quit

1-0000 5-	- <u>r</u> 3r4	Reference Data		<u>rr</u> —r9—
600780	256 Dec	611340	0910	Hex
600781	355 Dec	611341	0005	Hex
600782	5 Dec	61134Z	9962	Hex
600783	2000 Dec	611343	1155	Dec
699784	0 Dec	611344	360	Dec
600785	10 Dec	611345	2920	Hex
699786	10 Dec	611346	2920	Hex
600787	0 Dec	611347	0000	Hex
600788	0 Dec	611348	0100	Hex
		611349	0100	Hex
600790	256 Dec			
600791	355 Dec	611370	0010	Hex
600792	5 Dec	611371	0005	Hex
600793	2660 Dec	611372	0902	Hex
600794	0 Dec	611373	1155	Dec
600795	10 Dec	611374	360	Dec
600796	10 Dec	611375	292.0	Hex
600797	0 Dec	611376	2020	Hex
600798	0 Dec	611377	0000	Hex
		611378	0200	Hex
699660	256 Dec	611379	0200	Hex
600601	355 Dec			
Fornat (Decina)	1 Offline	Range 1		

Utility	Format 3	setting	Chylindu	Transfer	Template Disc	able	Quit
CDENU_5	-F3F	'4— lief	erence Dat	ta —	-17-Lov 8-16-0	JFF-	-19
600662	5	Dec	6114	90	0010	Hex	
600603	2000	Dec	6114	01	0005	Hex	
600604	0	Dec	6114	92	0002	Hex	
600605	10	Dec	6114	03	1155	Dec	
699886	10	Dec	6114	M	360	Dec	
600807	0	Dec	6114	95	2920	Hex	
699698	0	Dec	6114	96	2920	Hex	
			6114	97	0066	Hex	
600610	256	Dec	6114	96	0800	Hex	
600811	355	Dec	6114	919	0866	Hex	
600612	5	Dec					
600813	2000	Dec					
600614	0	Dec	6114	30	16	Dec	
600815	10	Dec	6114	31	1	Dec	
600816	10	Dec	6114	32	Z	Dec	
600617	0	Dec	6114	33	1154	Dec	
600618	0	Dec	6114	94	366	Dec	
600619	. 0	Dec	6114	35	1	Dec	
600620	0	Dec	6114	36	8	Dec	
600621	.0	Dec	6114	37	0	Dec	
Format (Decina)	00001	line	Bange	1			

Utility	Format	Setting	Chylindu	Transfer	Template Disa	ble	Quit
CDENO_5	-13	F4- list	ference Da	ta —	-17-Lev 8-16-0	JFF —	-19
500550	256	Dec	6106	50	3	Dec	1.2012
600551	355	Dec	6106	51	1	Dec	
600552	5	Dec	6105	52	Z	Dec	
600553	2000	Dec	6106	53	129	Dec	
699554	0	Dec	6106	54	1860	Dec	
600555	10	Dec					
699556	10	Dec					
600557	0	Dec					
			6106	60	3	Dec	
600560	256	Dec	6105	81	26	Dec	
600561	355	Dec	6106	82	. 2	Dec	
600562	5	Dec	6105	83	257	Dec	
600563	2000	Dec	6106	84	1801	Dec	
600564	0	Dec	1000				
600565	10	Dec					
600566	10	Dec					
600567	0	Dec					
600568	0	Dec					
600570	256	Dec	6107	10	3	Dec	
699571	355	Dec	6107	11	16	Dec	
600572	5	Dec	6107	12	Z	Dec	
E Fornat (Decina)	1 Of f	line	Bange	1			

Utility Format Setting ChyWadw Transfer Template Disable Quit

r1		Neference Data		Irr—r9——
600573	2660 Dec	610713	283	Dec
600574	0 Dec	610714	1827	Dec
600575	10 Dec			
600576	10 Dec	610740	3	Dec
699577	0 Dec	610741	4	Dec
699578	1 Dec	610742	Z	Dec
		619743	898	Dec
600580	256 Dec.	610744	1843	Dec
600581	355 Dec	610745	0	Dec
699582	5 Dec			
600583	2000 Dec			2
699584	O Dec			
600585	10 Dec	610770	3	Dec
600586	10 Dec	619771	2	Dec
699587	O Dec	610772	z	Dec
600588	1 Dec	610773	905	Dec
600589	257 Dec	619774	1847	Dec
100 E 30 E 20		610625	0	Dec
L Fornat (Decinal	Offline	Range 1		

Utility	Format	Setting	Chylindu	Transfer	Template Disa	ble	Quit
1	DENO_5F3	F4- list	ference Da	ta ——	-17-Lev 8-16-0	11 C	P9
11344		9 Dec	4136	6	8	Dec	
41345) Dec	4136	2	0.1	Dec	
41346	16256	Dec	4136	3	0 1	Dec	
41347		Dec .	4136	9	0 1	Dec	
41348	17466	Dec	4132	ð	ē 1	Dec	
41349		Dec	4137	£	0	Dec	
41350		Dec	4137	2	0.1	Dec	
11351	FP_BES_S-> 0	Dec	4137	3	0 1	Dec	
41352	() Dec	4137	£	0.1	Dec	
41353	<u>ે</u> (Dec	4137		0 1	Dec	
41354	C	Dec	4132		0.1	Dec	
41355	30	Dec .	4137	Z	0 1	Dec	
41356) Dec	4137	80	0 1	Dec	
41357		Dec	4137	9	0 1	Dec	
11358	<u>ે</u> () Dec	1138	9	0 1	Dec	
41359	C	Dec	4138	í	0.1	Dec	
41360		Dec	4138	2	0.1	Dec	
41361) Dec	4138		0.1	Dec	
41362		Dec	4138	4.	0.1	Dec	
41363) Dec	4138		01	0ec	
41364		Dec	4138	5	6 1	Dec	
41365	0	Dec.	4138	2	0 1	Dec	
Francet	(Berlinal) (00)	line	Barren	1			

Conclusion

As illustrated, the ladder logic is segmented according to the tasks required by the PLC. The tasks are:

- MSTR Modbus Plus Control
- XMIT Modbus Control of the Radio Modem Polling

- Operator Interface (MAGELLIS MMI) Control and Function Key Processing
- Calculation of Feeder Loading
- Completion of Line Sectionalizing Routines
- Subroutines to allow the PLC to easily calculate mathematics in floating point mathematics.

The ABB protective relay becomes a versatile device with the inclusion of common off the shelf equipment such as PLC's Operator interfaces such as MAGELIS and inexpensive radio modems. Building systems based upon solid communication protocols such as Modbus Plus (giving fast response to equipment communicating inside a substation) and Modbus (allowing efficient communication between devices at remote locations) allows complex systems to be added and engineered incrementally as a budget permits. Events occurring within the relay can easily be accessed. The easy to configure programming language within an Modicon PLC allows for additional automation capability to be added within a substation at minimal cost and minimal programming capability. It is easy to see why the use of PLC's and microprocessor relays is more prevalent in today's substation designs.

This program has been used with standard ABB product simulators. It was first presented in a joint Groupe Schneider and ABB seminar in 1998. Copies of this program may be obtained from ABB at no charge. It is intended for this program to serve as a guide for using PLC's and ABB IED's in automation systems. There is no expressed or implied warranty or any implication as to the accuracy of the logic and the content within.

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