Fast Recovery High-Power P-i-N Diode with Heavily Shorted Cathode for Enhanced Ruggedness in the Circuits with IGCTs

Libor Pína, ABB s.r.o., Semiconductors
Jan Vobecký, ABB Switzerland, Ltd. Semiconductors

Fast Recovery High-Power P-i-N Diode with Heavily Shorted Cathode for Enhanced Ruggedness in the Circuits with IGCTs

Libor Pína
ABB s.r.o., Semiconductors
Novodvorská 994, Prague 4, Czech Republic
libor.pina@cz.abb.com

Jan Vobecký
ABB Switzerland, Ltd. Semiconductors
Fabrikstrasse 3, Lenzburg, Switzerland
jan.vobecky@ch.abb.com

***Abstract*— We experimentally demonstrate that soft recovery of large area 4.5 kV Fast Recovery Diode (FRD) processed at thinner silicon can be achieved down to low temperature, if more than 50% cathode area is covered by shorts. The heavily shorted diode outperforms the classical one in the softness at DC link voltages well above the standard V_{DC} = 2.8 kV even with wafer thickness reduced by 15%. Parameter optimization results in the device with improved technology curve at T = 25 °C, comparable technology curve at T = 140 °C and unbeatable softness up to V_{DC} = 3.6 kV. Excellent switching ruggedness is shown for the worst case of high electron irradiation dose (the lowest E_{rec}), T = 25 °C and stray inductance of L_S = 600 nH.**

Keywords—component; formatting; style; styling; insert (key words)

I. INTRODUCTION

Switch-based Muli Level Converters for Medium Voltage range are dominated by 3-Level Neutral Point Clamped topologies. The state-of-the-art IGCTs and FRDs of 4.5, 5.5 and 6 kV voltage classes allow us to achieve the AC/DC efficiency of these inverters above 90 %. Further increase of the efficiency and performance / cost ratio requires the development of devices with lower losses. That of the FRD from the 4.5 kV IGCT/FRD chipset is presented below.

Overall losses of the FRD can be reduced using a thinner wafer, which is equipped with cathode shorts to avoid snappy reverse recovery. So far, the progress of FRDs with shorted cathode has been reported for chip diodes [1-4]. For the IGCT circuits with large-area discrete diodes, only the diodes with shorted cathode area up to 10% have been reported, which suffer from the snappiness at room temperature [5]. To eliminate this weakness, the shorted area between 25 and 75% is studied in this paper.

Beside the large area of discrete FRDs, resulting at very low current densities during the snap-off sweep down to zero current, the additional difficulty in the IGCT circuits is given by the di/dt choke $L_{di/dt}$. This choke is necessary for circuits with thyristor-like switches to limit the di/dt during turn-ON (see Fig.1a). The resulting voltage overshoots must be limited by clamping diode D_{CL}. As their magnitude depends on the stray inductance L_s of the clamping circuit, the tested FRD is typically exposed to higher voltage overshoots in comparison with the IGBT/IEGT circuits. The range of L_S = 170 - 600 nH used in this work covers the whole application range.

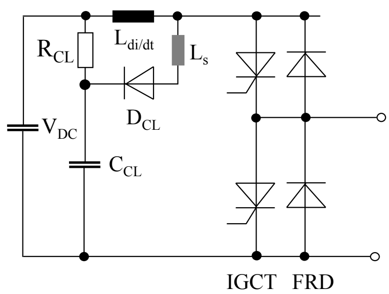

Fig.1a): Application circuit of FRD. Clamping circuit (R_{CL}, D_{CL} C_{CL}) limits the voltage overshoot caused by the di/dt choke $L_{di/dt}$. Stray inductance L_s may increase the voltage overshoot.

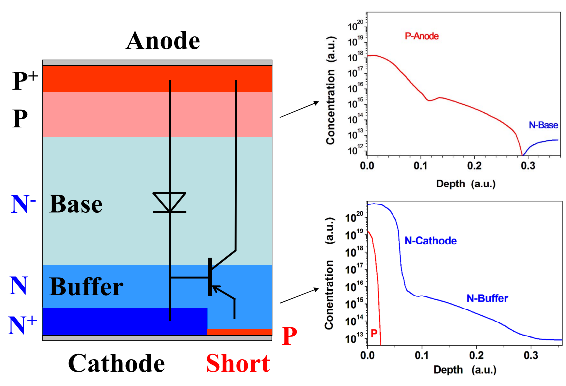

Fig.1b): FRD with cathode shorts (left). Doping profiles of anode and cathode (right). Anode doping profiles and lifetime control at the anode side are equal for all diodes in this work.

II. Device Design

The cathode short inserts an antiparallel PNP transistor into the original P-i-N diode structure (see Fig.1b). These transistors are designed for a maximal injection efficiency of holes from the cathode in the beginning of the tail phase of reverse recovery. However, this has to be done with caution, otherwise the original reverse blocking capability of the P-i-N diode might decrease and/or the excessive leakage current might degrade the blocking stability. As a logical consequence, the maximal junction temperature T_{jmax} would decrease. Since our goal is to maintain the T_{jmax} = 140 °C of the state-of-the-art FRDs, the design of the shorts is subordinated to the achievement of equivalent breakdown voltage and leakage current as in the FRD without shorts. The design of shorts is therefore subjected to trade-off between the static parameters (breakdown voltage, leakage current, forward voltage drop) and reverse recovery losses and softness.

According to the ref. [5], the softness of the shorted FRDs decreases with decreasing operation temperature. This is because the rest of stored charge from the ON-state, which polarizes the p-n junction “P-short-N-buffer” into forward direction to inject holes for a softer recovery, decreases with decreasing temperature. The only way to assure the soft recovery at minimal rated operation temperature is therefore the choice of a proper short size and the coverage of cathode by these shorts. To find the optimum which satisfies this requirement, the FRDs with shorted cathode area of 25, 50 and 75 % and different short sizes have been tested under various circuit conditions. Fig.2 illustrates the appearance of the shorts with various cathode area coverage.

Fig.2: Cathode area coverage by hexagonal P-type shorts is 25, 50 and 75%.

The wafer thickness, N-buffer, N^+-emitter and P-type short doping profiles from Fig.1b) have been optimized in the loop: breakdown voltage → leakage current → technology curve → RB SOA (I_{min}, I_{max}, V_{DCmax}, L_{Smax}). The wafer thickness is by 10 to 15 % lower than that of the *Classical* devices without shorts (references) in order to improve the technology curve between the ON-state and turn-off losses V_F - E_{rec}. The original breakdown voltage has been preserved. The effect of the inserted PNP transistor on the increase of leakage current has been minimized.

III. Experimental Results

The technology curves of the *Classical* and *New* diodes are shown in Fig.3. For given dose of electron irradiation (EI), the *New* device with 75 % short coverage has always a higher V_F and lower recovery losses E_{rec} than the *Classical* one due to the reduced N-type cathode area injecting the electrons in the ON-state. The situation for V_F with 25 % coverage is just opposite, while the break-even point is at about 50 %. The benefit of the

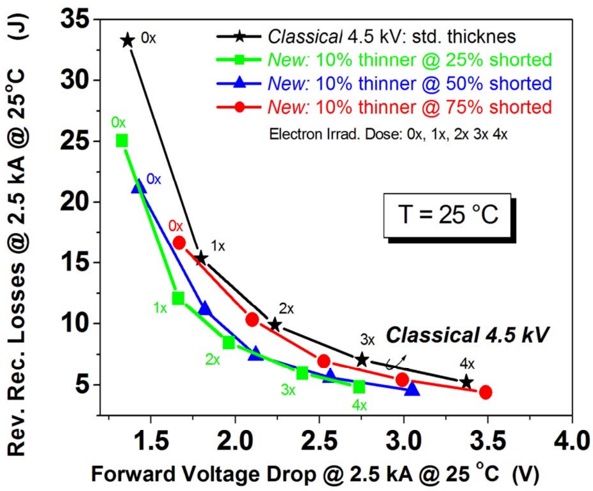

Fig.3a): Technology curves of 4.5 kV *Classical* and *New* FRDs measured at room temperature by changing the dose of EI (*0x* marks the unirradiated device).

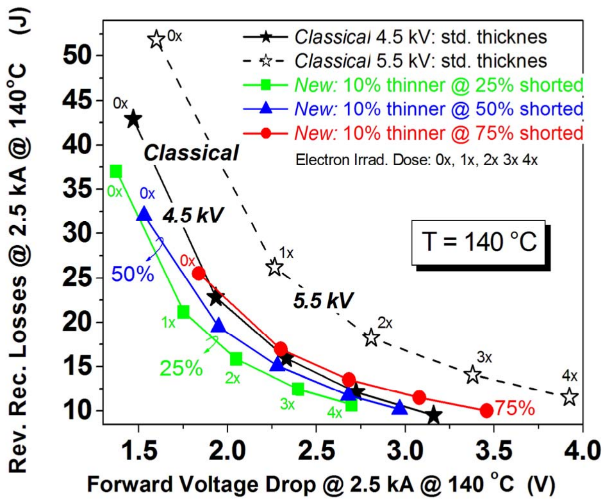

Fig.3b): Technology curves of 4.5 kV and 5.5 kV *Classical* and 4.5 kV *New* FRDs measured at T = 140 °C.

new technology then depends on how much amounts the E_{rec} for given EI dose and operating temperature.

At room temperature, the technology curves of the *New* diodes are better than that of the *Classical* one regardless of the coverage by shorts. The *New* diode profits from the reduction of thickness, which results in less stored charge at the cathode side in the ON-state and hereby at a lower tail charge and E_{rec} compared to the *Classical* device. As illustrated in Fig.4a), this advantage vanishes for the coverage of 75% and the highest EI dose, where the *Classical* and *New* devices achieve nearly identical E_{rec}.

At T = 140 °C, the benefit from the 10 – 15 % reduced wafer thickness in favor of technology curve is decreased for the shorted area of 25 – 50 %. The coverage of 75 % gives the worst technology curve for high EI doses. The comparison of Figs.3a) and b) shows that the voltage drop of the *New* device

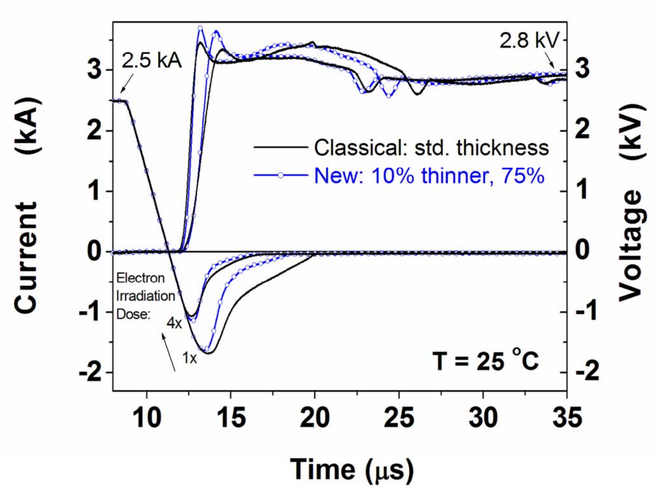

Fig.4a): Reverse recovery of 4.5 kV *Classical* and *New* FRDs measured at room temperature for the lowest (*1x*) and highest dose of electron irradiation (*4x*). The *New* FRD has 75% cathode coverage by shorts.

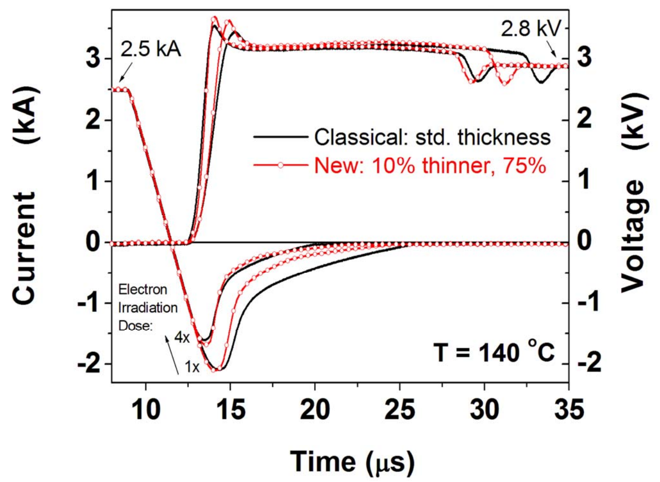

Fig.4b): Reverse recovery of 4.5 kV *Classical* and *New* FRDs measured at T = 140 °C for the lowest (*1x*) and highest dose of electron irradiation (*4x*).

is practically independent of operation temperature at 2.5 kA. It is therefore the more increased E_{rec} of the *New* diode with temperature compared to the *Classical* one, which worsens the technology curve at T = 140 °C (see Figs.4a) and b)). Reason is the increased injection from the P-type shorts at high temperature, respectively the increased current amplification of the P-N-P transistor. As a result, the tail current increases, the tail time gets longer and the E_{rec} significantly increases as well. In general, the better softness down to low operation temperature implies the higher E_{rec}.

Figs.5 and 6 show the worst case softness (L_s = 600 nH, EI dose 4x) achieved at the reverse recovery with the DC link voltages V_{DC} = 2.8 kV and V_{DC} = 3.6 kV. V_{DC} = 2.8 kV represents the industry standard for the 4.5 kV class, V_{DC} = 3.6 kV the overvoltage conditions for the 5.5 kV one.

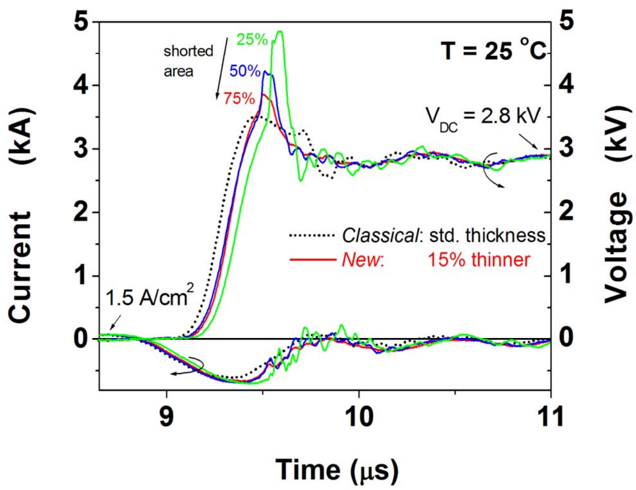

Fig.5a): Reverse recovery at V_{DC} = 2.8kV and J_F = 1.5A/cm^2 measured at room temperature for L_s=600nH and EI dose 4x.

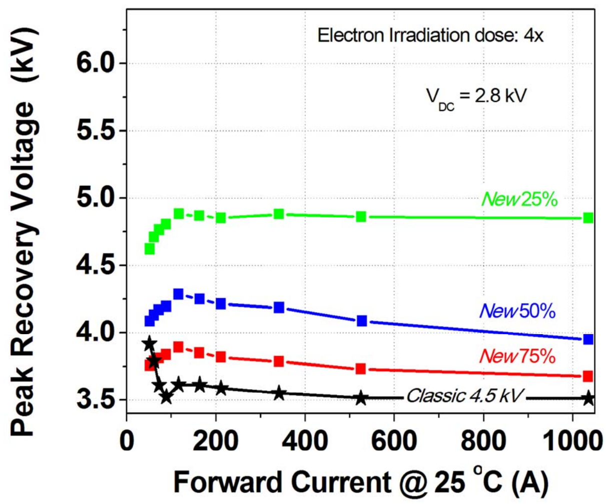

Fig.5b): Peak recovery voltage vs. ON-state current for the conditions from Fig.5a). The *Classic* device is softest in the whole range of low currents. The *New* FRD must be ≈75 % shorted to achieve similar softness for L_s = 600nH below 100 A.

The *Classic* diode, the thickness of which is optimized for the V_{DC} = 2.8 kV, shows the lowest peak recovery voltage V_{pkr} down to 75 A (see stars at Fig.5b). Below this current, the V_{pkr} shows steep growth with decreasing current as a result of practically zero tail current. The *New* diodes are by 15 % thinner and to reduce the peak recovery voltage V_{pkr} below the rating voltage of 4.5kV, the shorted area must be ≥ 50% for L_s=600 nH. They show a higher V_{pkr} down to 100 A. but they are superior below 75 A over the *Classic* one. Typical applications have the stray inductance about one half of the presented case so that both the *Classic* and *New* diodes satisfy our needs.

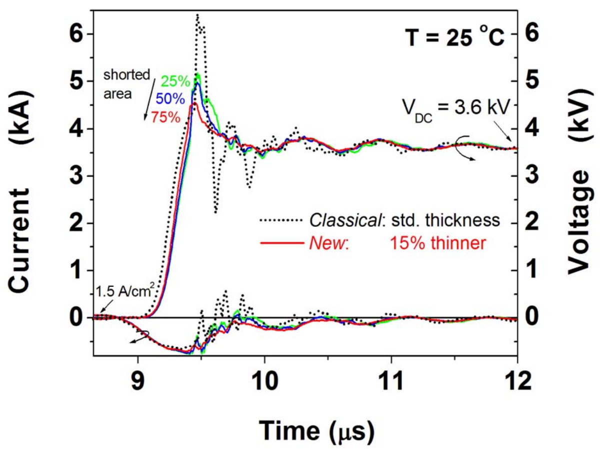

Fig.6a): Reverse recovery at V_{DC}=3.6kV and J_F=1.5A/cm^2 measured for the worst case: L_s=600nH and EI dose 4x.

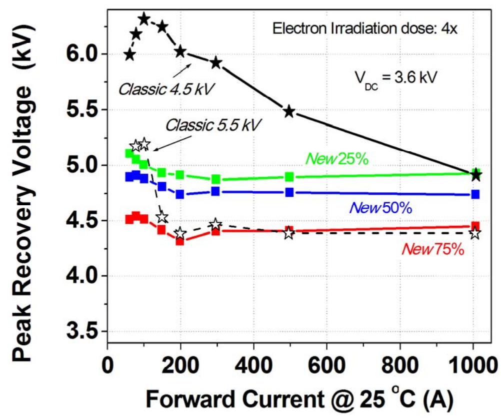

Fig.6b): Peak recovery voltage vs. ON-state current for the conditions from Fig.6a).

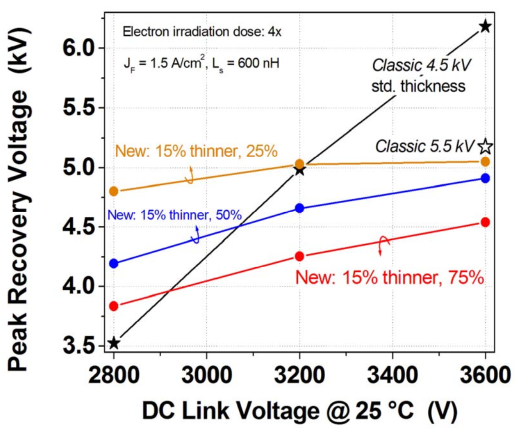

Fig.7: Peak recovery voltage vs. DC link voltage. Capability of the *Classic* 5.5 kV diode is shown only for V_{DC} = 3.6 kV (open star).

For V_{DC} = 3.6 kV, the V_{pkr} of the *Classic* 4.5 kV diode was measured much higher than the typical static breakdown voltage of 5.6 kV (Fig.6a)). No failure has appeared only due to a special provision in our test circuit. Fig. 6b) shows that the *Classic* 4.5 kV FRD is the most snappy of all presented devices and that even the *Classic* 5.5 kV device snaps below 200 A. On the other hand, the cathode short coverage of 75% results in $V_{pkr} \leq$ 4.5kV down to zero current. The voltage overload capability at low current density goes to extreme.

Fig.7 shows the sensitivity on the DC link voltage. Safe operation of the *Classic* FRD is limited below 3.2 kV for the presented case of L_S = 600nH. Safe operation up to V_{DC} = 3.2 kV is possible with a lower L_s, typically around 300 nH. Physical reason for this behavior is the missing stored charge at the cathode side at the tail phase when the diode current drops to zero. As the *New* diode injects the required charge in the tail time by the P-type shorts, the sensitivity on the DC link voltage is minimized. Consequently, the *New* FRD shorted to 75 % operates safely ($V_{pkr} \leq$ 4.5 kV) up to V_{DC} = 3.6 kV. For L_s = 170nH, even the *New* diode with 50% shorted area satisfies the limit of $V_{pkr} \leq$ 4.5 kV (not shown here). On the other hand, the 5.5 kV *Classic* diode (dashed line), which is much thicker than the 4.5 kV *Classic* one, is snappier than the weakest diode from all the *New* ones at V_{DC} = 3.6 kV.

IV. CONCLUSIONS

Fast recovery 4.5 kV diode with cathode shorts was optimized for ultimate softness at T = 20 - 140 °C, $V_{DC} \leq$ 3.6 kV and L_s = 170 - 600 nH. The dense shorting pattern raises the reverse recovery softness of the *New* 4.5 kV FRD above that of the *Classical* 5.5 kV class even for 15% thinner silicon. At elevated temperatures, the shorts increase the recovery losses so that the benefit from wafer thinning for technology curve vanishes. This can be changed by optimization for the lowest losses resulting in a slight decrease of the softness.

ACKNOWLEDGMENT

We acknowledge the support of K. Stiegler, S. Deore and M. Waldman in processing of experimental devices.

REFERENCES

[1] K. Satoh, K. Morishita, Y, Yamaguchi,N. Hirano, H. Iwamoto, A. Kawakami, Proceedings of ISPSD´2000, Toulouse, pp. 249 – 252, 2000.

[2] A. Kopta, M. Rahimo, Proceedings of ISPSD´2005, Santa Barbara; pp. 83 – 86, 2005.

[3] F. Masuoka, K. Nakamura, A. Nishii, T. Terashima, Proceedings of ISPSD´2012, Bruges, pp. 373 – 376, 2012.

[4] S. Matthias, S. Geissmann, M. Bellini, A. Kopta, M. Rahimo, Proceedings of ISPSD´2013, Kanazawa, pp. 335 – 338, 2013.

[5] L. Pina, J. Vobecky, *Microelectronics Reliability* 53, pp. 681 – 686, 2013.