The 150 mm RC-IGCT: a Device for the Highest Power Requirements

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***Abstract*—A 4500V RC-IGCT switching more than 10 kA in both switch and diode mode was developed for application in cascaded multilevel topologies. The performance was facilitated by using most of a 150 mm silicon wafer for a single device. Furthermore, the stray inductance of the gate bushing inductance was lowered an order of magnitude, and the use of an outer ring gate contributed significantly to lower impedance on the device itself. Adjustment of the di/dt choke led to significant reduction of total losses. FCE as a means of loss optimization was investigated.**

I. INTRODUCTION

The Reverse-Conducting Integrated Gate Commutated Thyristor (RC-IGCT) is a monolithic integration of an IGCT switch [1] with an antiparallel diode in a high contact force "hockey-puck" ceramic package. The integration provides a compact building block for voltage-source inverters, like IGBT modules. Unlike IGBTs, the IGCT operates like a thyristor in the on-state which gives it an advantage in intrinsic loss generation. The IGCT turn-off speed cannot be controlled intrinsically therefore an overvoltage–clamped dI/dt choke is typically used in application. For the semiconductor device this leads to the advantage that the turn-on losses can be kept very low.

The IGCT is particularly well-suited for low frequency applications thanks to its low on-state voltage drop. The cascaded multilevel topology converter [2] makes this possible while facilitating arbitrarily high[1] converter voltage rating by adding more levels. A further advantage for the IGCT in that it fails short reliably [3], which eases inclusion of redundant levels. The power handling capability of the developed device in this topology allows for the highest power requirements to be met. Specifically, network applications such as reactive power compensation, High-Voltage-DC transmission or as the network interface inverter for hydro-static energy storage pumps / generators are targeted; applications for which the power rating can reach gigawatts and typical voltage requirements vastly outnumber today's semiconductor ratings.

[1] Independent on semiconductor voltage rating or need for their series connection.

II. FABRICATED STRUCTURE

A. *Silicon device*

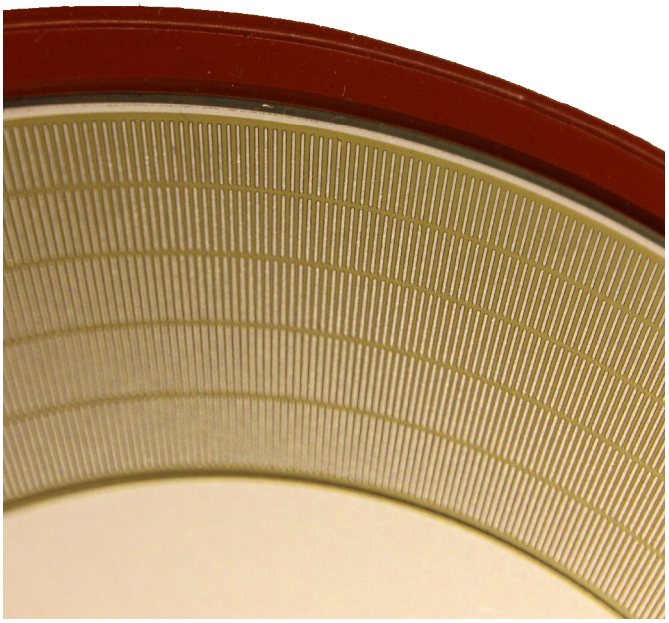

Figure 1. A photograph of the produced wafer showing (bottom to top) the diode in the centre, the separation region, five rings of GCT segments, the ring-formed gate contact area and the silicon rubber around the edge of the wafer.

The HPT+ technology platform [4], initially developed for asymmetric devices, was modified to allow for integration of an antiparallel diode. In particular, the diode and GCT p-diffusions were separated spatially in order to accommodate reverse-biasing the diode between gate and cathode. A photograph of the wafer is shown in figure 1. The vertical

structure is shown in fig. 2. The silicon starting material was chosen to result in less than 100 FIT due to cosmic rays at 2.8kV constant anode voltage.

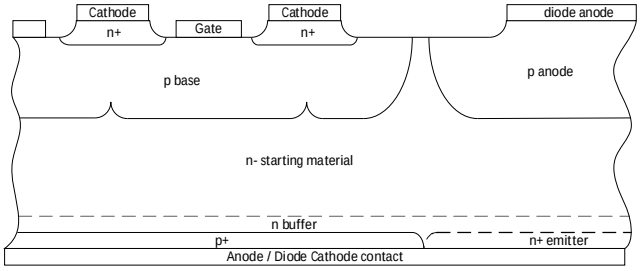

Figure 2. A cross-section through the silicon wafer showing the vertical structure, taken around the separation region between GCT and diode parts.

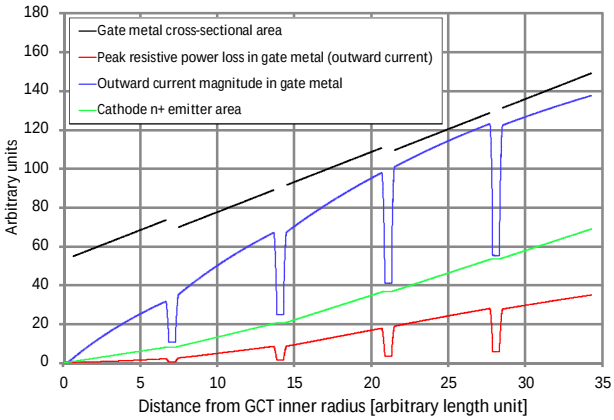

Figure 3. A comparison of the gate metal properties of the asymmetric device with inner ring gate made on 100 mm wafers and the developed device with outer ring gate made on 150 mm wafers.

Gate signal propagation is of high importance for the controllable current of the IGCT, and the importance increases as the device area gets larger. Applying an outer ring gate to the wafer instead of an inner ring gate has two important effects. On one hand, the distance that the current has to flow on the wafer increases, but the distance lost on the wafer is gained in the gate lead. On the other hand, and more importantly, the cross-sectional area of the gate metalisation increases in the same direction as the current increases. Figure 3 shows the result of a simulation of the gate metalisation for our design. The gate current increases from the most gate-contact distant area proportionally to the accumulated segment area. The conduction of this gate current is the responsibility of the gate metal sheet, roughly the distance between segments. The resulting gate metal power, peak resistive loss density during maximal gate current could be reduced by almost 80% compared to a current 100 mm design, in spite of the current being around twice as high in the larger device.

B. Integration with gate unit

IGCT operation depends on the ability to commutate the entire current from the cathode to the gate before the anode voltage starts to rise – the so-called hard-drive limit. The time available for this transition is the same for any device size and current rating. A commonly used order of magnitude for it is a microsecond, but in reality it is much less. Hence, stray inductance minimisation increases in importance with device size and current rating. In order to scale the controllable current up sufficiently, a new gate bushing for the hermetic housing was developed. The principle is to avoid separating the gate and auxiliary cathode flanges of the GCT housing, even at the cost of a longer gate lead, in order to save on inductance. The developed housing is estimated to have a stray inductance of around 200 pH at 1 MHz, to be compared to 1.6 nH of the previous generation of housing.

C. Diode options

Using one and the same pressure contact for both switch and diode limits the choice of silicon starting material to one thickness. The switching behaviour – snap-off eagerness – is more critical for the diode than for the IGCT. The thermal stress, on the other hand, is usually more critical for the IGCT. As a result, efficiency and power handling capability requirements of the IGCT tend to drive the silicon thickness to the absolute minimum while maintaining a reasonable snap-off-free diode. Hence, technologies that allow for decreasing the diode thickness like FCE [5] and double peaks of ion-irradiation [6] are welcome contributions to improve the rating of the combined device. A working FCE function is necessary for achieving an acceptable diode behaviour with a silicon thickness that suffices for the GCT part – even with a stray inductance below 100 nH. It is necessary to balance the buffer implantation dose between stopping the electric field before punch-through to the GCT anode, and lateral resistivity over the FCE shorts. We have found this balance to be favourable between $5 \cdot 10^{12}$ and $1 \cdot 10^{13}$ ions per square centimetre.

D. Gate unit

The gate unit design was altered to fit the larger housing and the capacitance and switches of the turn-off channel were scaled to accommodate a turn-off current of more than 10kA. As the stray inductance in the six-layer printed circuit board is significantly lower than the one of the gate lead and bushing – around 90 pH, nor further optimisation was necessary.

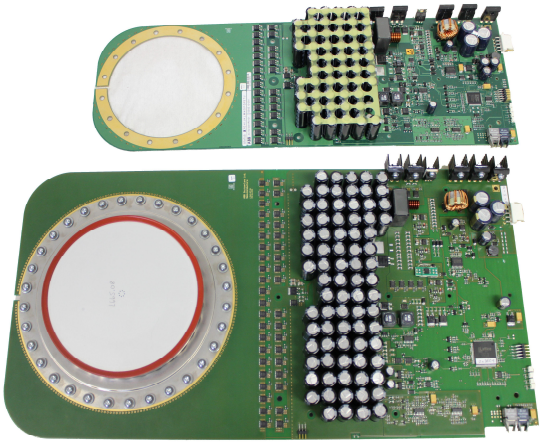

Figure 4. The developed gate-unit (bottom) together with a gate unit for use with today's 100 mm devices (top)

III. Switching Circuit

The cascaded multilevel topology can be realised with an infinite number of different circuits for the individual levels. For this device, the clamped and choked half-bridge for evaluating the behaviour of the device was used. The circuit is shown in figure 4. The size of the diode, around for decreasing the dI/dt choke significantly compared to circuits based on 100 mm RC-IGCTs. The diode can be switched at above 2kA/ms without risking failure. This translates to a dI/dt choke inductor in the range of one to two microhenries. This inductance value can easily be constructed by means of the bus bars alone. Moreover, since the energy stored in the choke inevitably ends up heating the clamp resistor at both GCT and diode turn-off, decreasing the size of the inductor has a significant and positive influence on the total efficiency of the circuit.

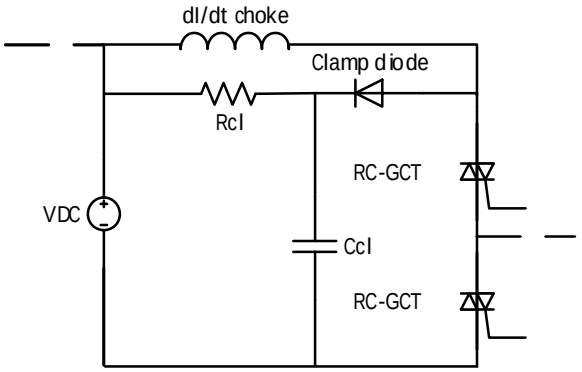

Figure 5. The electric circuit used for device evaluation – the half-bridge with an over-voltage clamped dI/dt choke.

IV. Electrical Results

The electrical testing consisted of static measurements of on-state and blocking properties – these results are shown in figures 6 through 8.

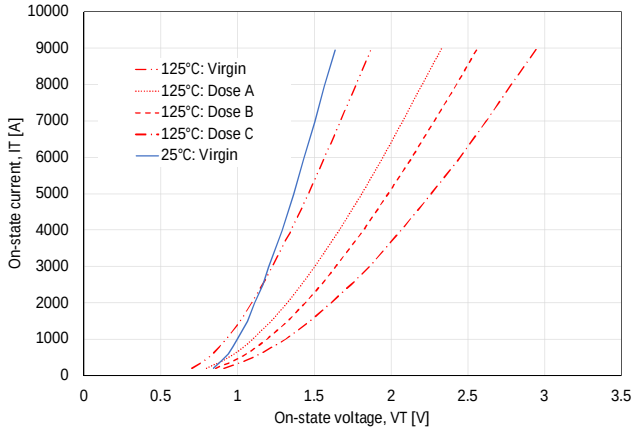

Figure 6. On-state IV-characteristics of the GCT part at different levels of lifetime reduction through electron irradiation.

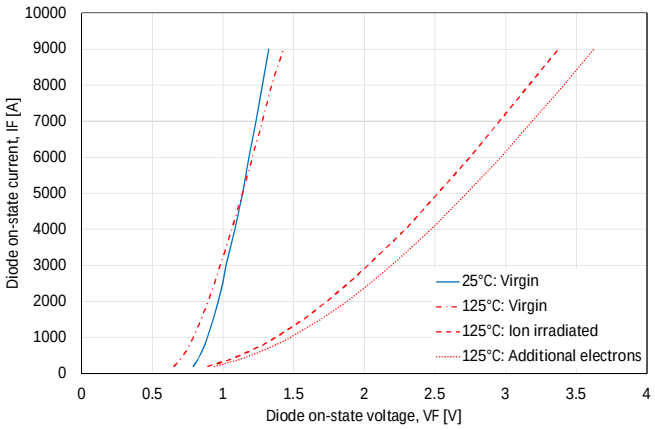

Figure 7. On-state IV charactersitcs of the diode part before and after heavy ion irradiation

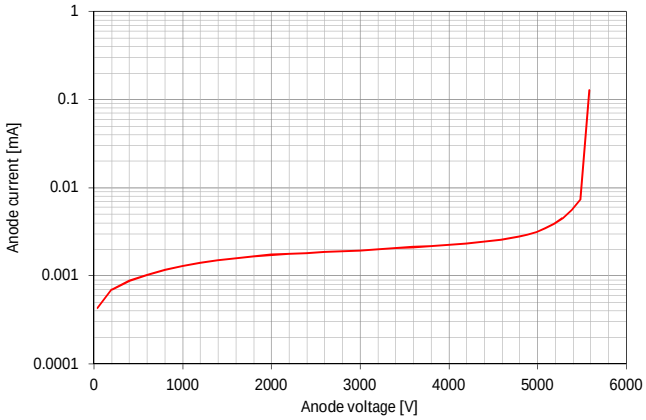

Figure 8. Off-state current-voltage characteristics at 25°C

The dynamic turn-off losses, or the trade-off curves are shown in figure 9. The influence of reducing the dI/dt choke inductor to allow higher diode switching speed is shown in figure 10. The total losses, for the assumed conditions, could be reduced by 15%.

The safe operation limits in terms of maximal controllable current and were investigated in destructive tests; for the GCT part, the highest current that was turned off amounted to some 9500A at 125°C, and beyond 10000A at room temperature (not shown). In addition, a test of the hard-drive limit, or the limit of the gate-unit combined with the gate circuit stray impedance, was conducted.

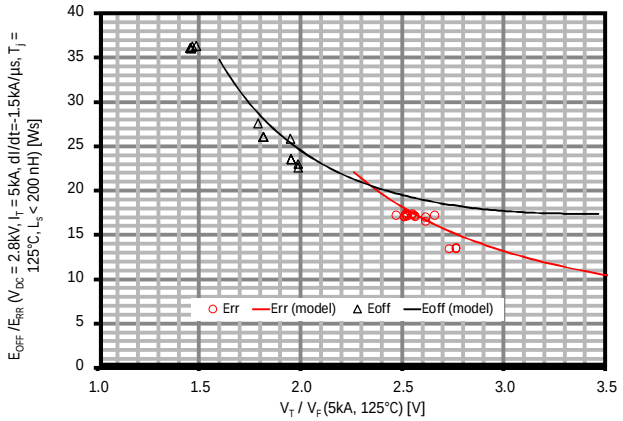

Figure 9. Trade-off of dynamic and static losses for both GCT and diode parts at 125°C and 5kA. Even at 5kA, an on-state voltage as low as 1.5 V is achievable for the switch

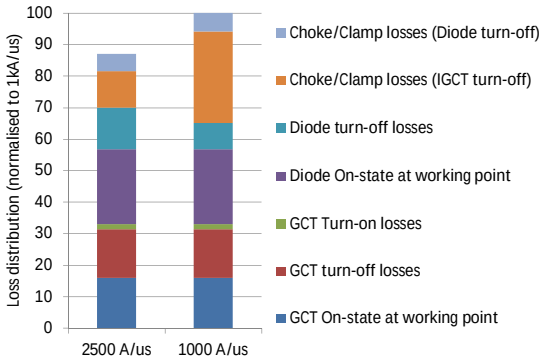

Figure 10. Demonstration of loss benefit when increasing diode switching speed of 1000A/µs to 2500A/µs.

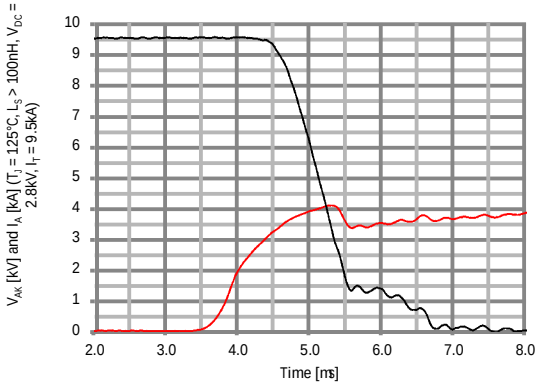

Figure 11. Demonstration of the maximal controllable current of the GCT part at 125°C

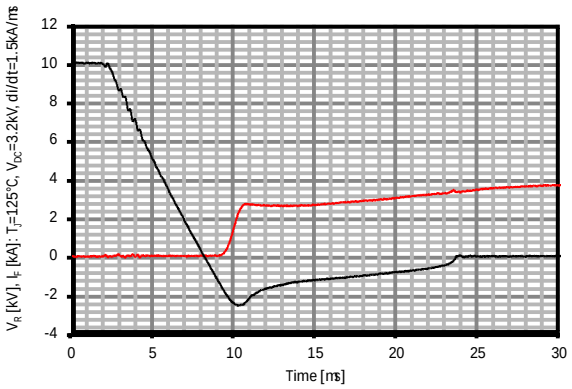

Figure 12. Demonstration of Diode-Part SOA at 3.2kV and 125°C

V. Conclusion

A reverse conducting IGCT for applications with the highest power requirement was developed and demonstrated. It can be used for DC-link voltages up to 2.8kV and and is able to handle currents up to 9.5kA. The component is especially well-suited for modular multi-level topologies with voltage-source cells, thanks to the low on-state voltage.

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